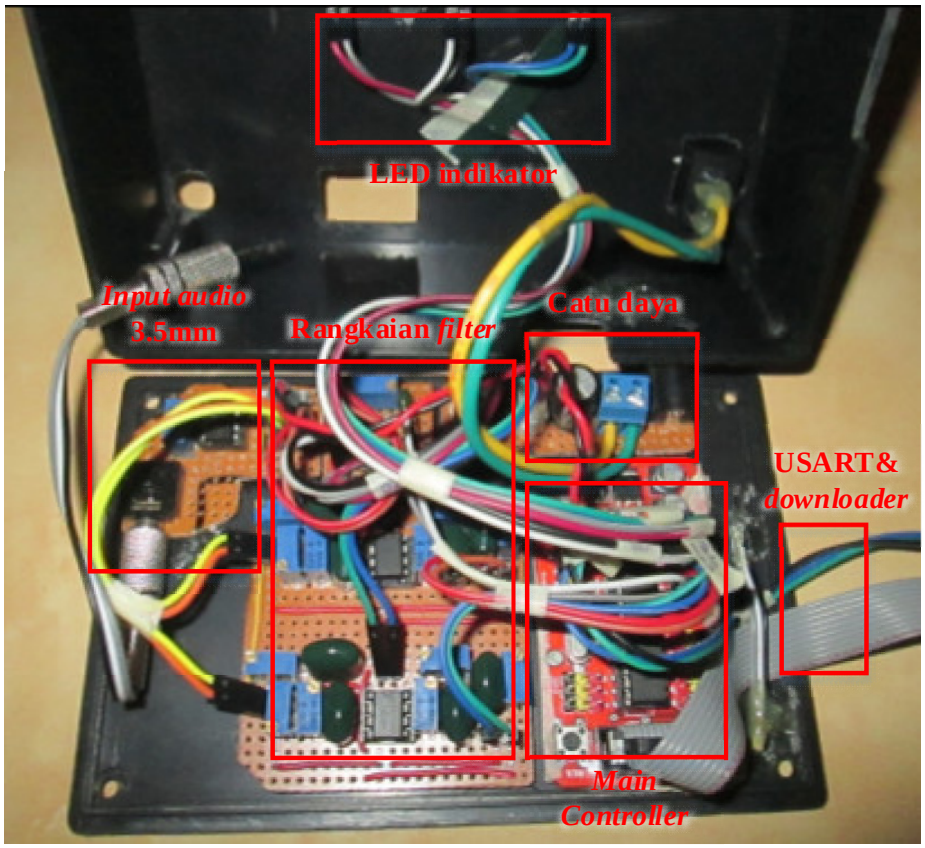
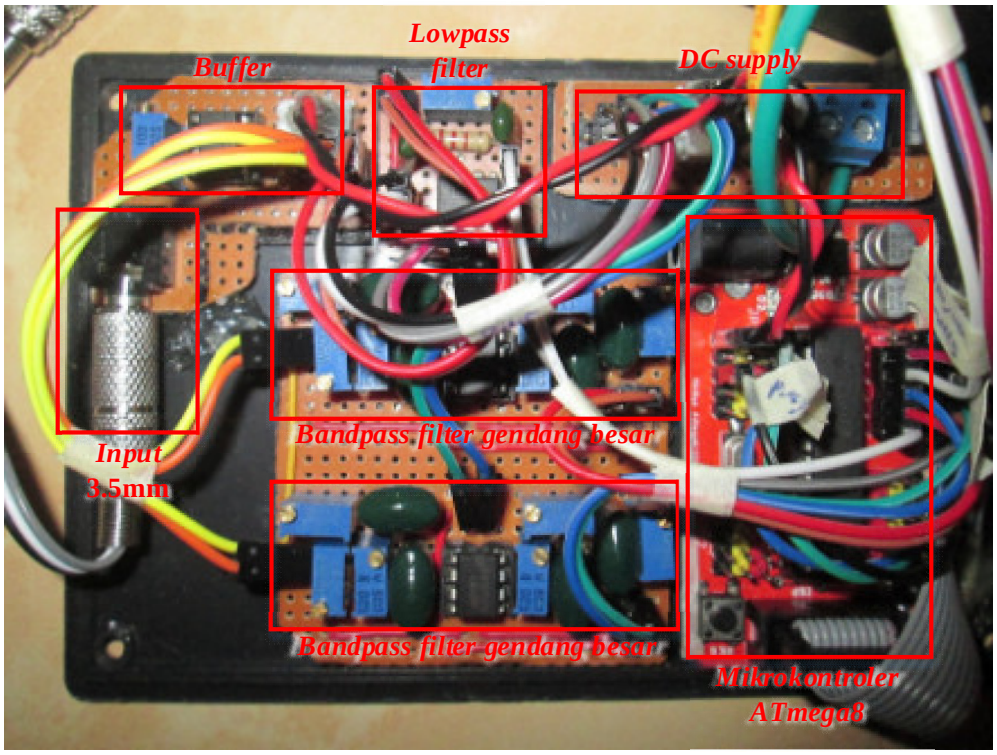
LAMPIRAN 1
DOKUMENTASI ALAT

Gambar 1. Foto alat tampak depan

Gambar 2. Foto alat tampak atas



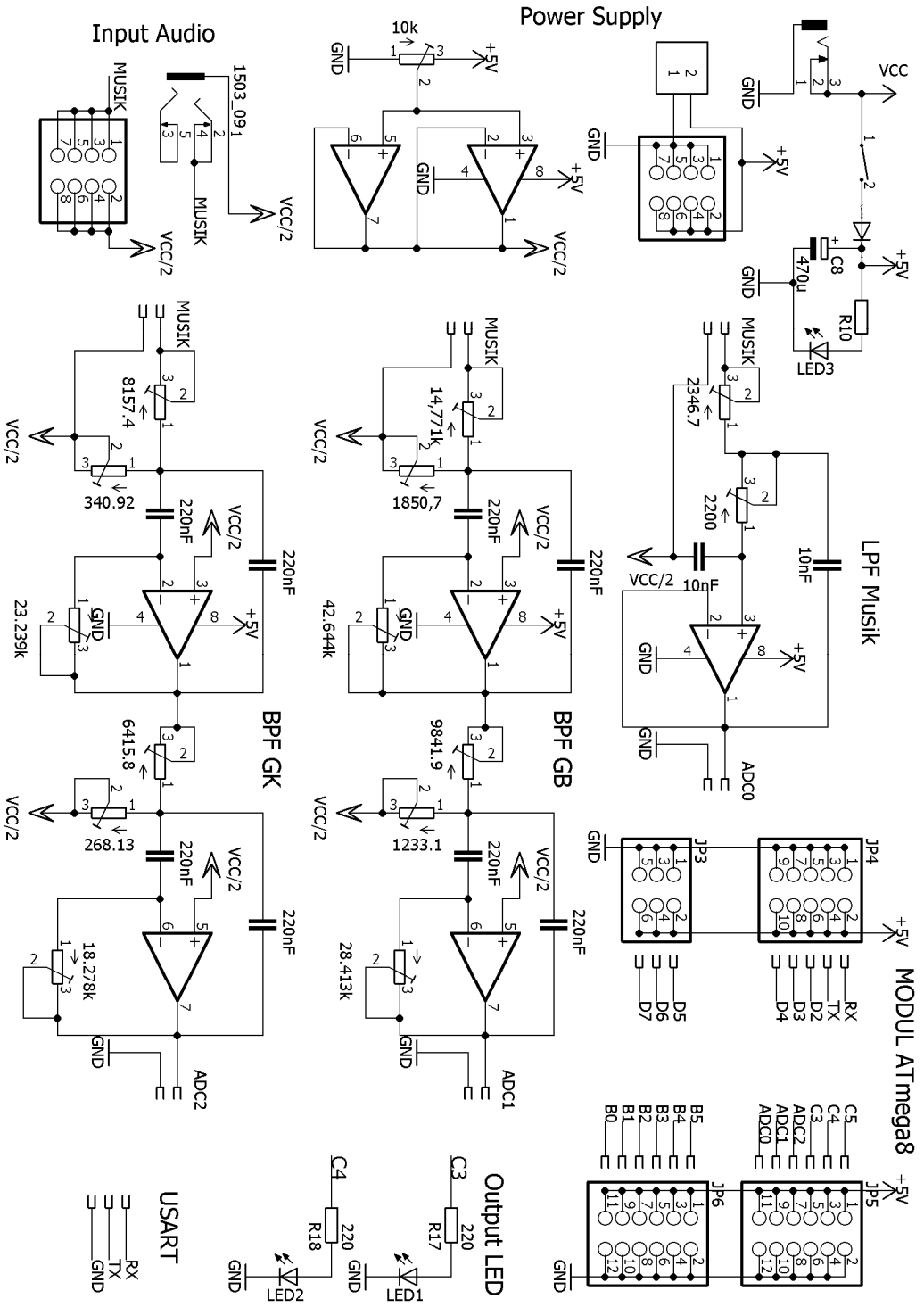
Gambar 3. Foto alat bagian dalam



Gambar 4. Rangkaian elektrik keseluruhan

LAMPIRAN 2

SKEMATIK RANGKAIAN



Gambar 5. Skematik Rangkaian Keseluruhan

LAMPIRAN 3
LISTING PROGRAM

```
#include <mega8.h>
#include <delay.h>
#include <stdio.h>
#define ADC_VREF_TYPE 0x00

// AD Conversion
unsigned int read_adc(unsigned char
adc_input)
{
ADMUX=adc_input | (ADC_VREF_TYPE &
0xff);
// Delay needed for the stabilization of the
ADC input voltage
delay_us(10);
// Start the AD conversion
ADCSRA|=0x40;
// Wait for the AD conversion to complete
while ((ADCSRA & 0x10)==0);
ADCSRA|=0x10;
return ADCW;
}

//Global Variables
//Referensi ADC
#define refAtasADC0 383
#define refBawahADC0 377
#define refAtasADC1 402
#define refBawahADC1 358
#define refAtasADC2 408
#define refBawahADC2 352
//Logic output
#define ADA 1
#define TIDAK_ADA 0

//Deteksi Lagu
int inADC0;     //input deteksi lagu 50ms
int outADC0; //output untuk keputusan
deteksi lagu 50ms
int resADC0_Ada[10]; // Tidak ada > ada
250ms
int resADC0_Tidak[20]; //Ada lagu > mute 2s
int flagSuara; //output deteksi lagu
//Deteksi Gendang
int inADC1; //input ADC gendang besar 10ms
int inADC2; //input ADC gendang kecil 10ms
int outADC1, outADC2; //output logic untuk
keputusan deteksi 10ms
int sampADC1[10]; //Deteksi gendang besar
pada periode 50ms
int sampADC2[10]; //Deteksi gendang kecil
pada periode 50ms
int outsamp1, outsamp2; //output deteksi
gendang untuk pola musik 50ms

//Deteksi Pola Musik 1000ms
int resADC1[20]; //input deteksi gendang
besar
int resADC2[20]; //input deteksi gendang
kecil
int flagPola; //output pola musik

//Counter untuk array
int nA=0; //pada proses1 untuk proses2
int nB=0; //pada proses1 untuk proses6
int nC=0; //pada proses3 untuk proses4
int nD=0; //pada proses4 untuk proses5

//Sampling ADC Musik pengiring 50ms
void proses1()
{
inADC0 = read_adc(0);
//printf("%d ",inADC0);
if ((inADC0>=refAtasADC0)
||(inADC0<=refBawahADC0))
      { outADC0=ADA; }
else { outADC0=TIDAK_ADA; }
//Memasukkan outputADC0 ke array
```

```
resADC0_Ada[nA]= outADC0;
resADC0_Tidak[nB]= outADC0;
nA++;
nB++;
}

//Deteksi adanya suara musik  250ms
void proses2()
{
if(flagSuara==TIDAK_ADA)
{
int cntNyala = 0;
for(nA=0; nA<5; nA++)
      {
      if (resADC0_Ada[nA]==ADA){
      cntNyala++;    }
      }
if(cntNyala>=3)    flagSuara= ADA;
      }
nA=0;     }

//Deteksi adanya mute   1000ms
void proses3()
{
if (flagSuara==ADA){
int cntMute=0;
for(nB=0; nB<20; nB++)
      {
      //hitung jumlah mute
      if (resADC0_Tidak[nB]==TIDAK_ADA)
      { cntMute++;  }
      }
//Penentuan keputusan Apakah Mute?
if(cntMute>=18) {
      flagSuara= TIDAK_ADA;        }
    }
nB=0;     }

//Sampling ADC Gendang  10ms
void proses4()
{
inADC1= read_adc(1);
inADC2= read_adc(2);
//printf("%d,%d ", inADC1, inADC2);

//deteksi ada gendang besar
if ((inADC1>=refAtasADC1)||
(inADC1<=refBawahADC1)){
      outADC1=ADA;      }
else { outADC1=TIDAK_ADA;       }

//deteksi ada gendang kecil
if ((inADC2>=refAtasADC2)||
(inADC2<=refBawahADC2)){
      outADC2=ADA;      }
else {      outADC2=TIDAK_ADA;  }

//if(flagSuara==ADA) printf("%d,%d
",inADC1, inADC2);
//else    printf("xxx ");

//Memasukkan outputADC1 dan
outputADC2 ke array
sampADC1[nC]= outADC1;
sampADC2[nC]= outADC2;
nC++;     }

//Hasil gendang dalam periode 50ms
void proses5()
{
if(flagSuara==ADA)
{
int cntGB1= 0;
int cntGK1= 0;
//proses hitung adanya gendang pada
sample ke- n
for(nC=0; nC<5; nC++)
      {
      if (sampADC1[nC]==ADA){
      cntGB1++;     }
      if(sampADC2[nC]==ADA){
      cntGK1++;     }
      }
//printf("%d,%d ", cntGB1, cntGK1);
//keputusan deteksi gendang
if(cntGB1>=2) {      outsamp1= ADA;   }
else {      outsamp1= TIDAK_ADA;      }
if(cntGK1>=2) {      outsamp2= ADA;   }
else {      outsamp2= TIDAK_ADA;      }
nC=0;
```

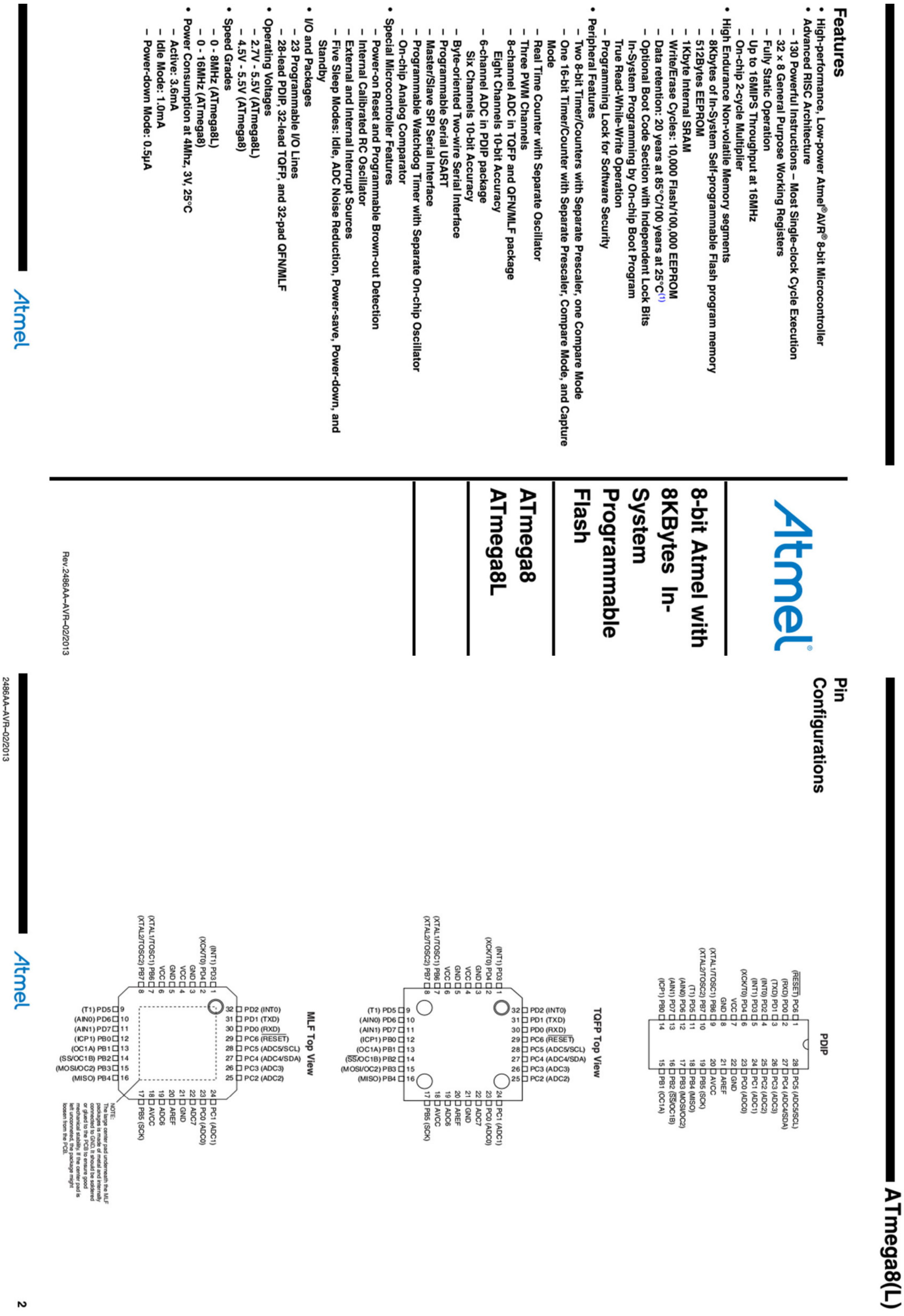
```
//Memasukkan outsamp1 dan outsamp2 ke
array
resADC1[nD]= outsamp1;
resADC2[nD]= outsamp2;
nD++;
}
}

//Deteksi Pola Musik Pengiring 1000ms
void proses6()
{
if (flagSuara==ADA)
{
int cntGB2=0;
int cntGK2=0;
//proses hitung ada gendang sample ke- n
for(nD=0; nD<19; nD++)
      {
      if (resADC1[nD]==ADA){
      cntGB2++;     }
      if (resADC2[nD]==ADA){
      cntGK2++;     }
      }
//printf("%d,%d ", cntGB2, cntGK2);
//Keputusan Apakah ada Pola musik?
if((cntGB2>=4)&&(cntGK2>=4))
      {     flagPola=ADA;       }
else { flagPola=TIDAK_ADA;  }
}
nD=0;
}

//Pengiriman data USART
void proses7()
{
if(flagSuara==ADA)
{
//printf("%d,%d ", outsamp1, outsamp2);
printf("%d,%d,%d ", flagPola,outsamp1,
outsamp2);    }
else
{
//printf("X,X ");
//printf("x,x,x ");    }
//printf("%d", flagSuara);     }

//Indikator Sistem dan Pola
void proses8()
{
//Indikator Sistem Aktif
if(flagSuara==ADA)    PORTC.3=1;
else    PORTC.3=0;
//Indikator ada Pola Musik
if(flagPola==ADA)    PORTC.4=1;
else    PORTC.4=0;         }

void main(void)
{
int cnt1=0; //Cnt sampling ADC0 50ms
int cnt2=0; //Cnt deteksi ada Lagu 250ms
int cnt3=0; //Cnt sampling ADC1 ADC2 10ms
int cnt4=0; //Cnt deteksi gendang 50ms
int cnt5=0; //Cnt deteksi pola musik 1000ms
int cnt6=0; //Cnt deteksi ada Mute 2000ms
int cnt7=0; //Cnt kirim data USART

// Input/Output Ports initialization
// Port B initialization
// Func7=In Func6=In Func5=In Func4=In
Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T
State3=T State2=T State1=T State0=T
PORTB=0x00;
DDRB=0x00;
// Port C initialization
// Func6=In Func5=In Func4=Out Func3=Out
Func2=In Func1=In Func0=In
// State6=T State5=T State4=0 State3=0
State2=T State1=T State0=T
PORTC=0x00;
DDRC=0x18;
// Port D initialization
// Func7=In Func6=In Func5=In Func4=In
Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T
State3=T State2=T State1=T State0=T
PORTD=0x00;
DDRD=0x03;
// Timer/Counter 0 initialization
// Clock source: System Clock
// Clock value: Timer 0 Stopped
```

```
TCCR0=0x00;
TCNT0=0x00;

// Timer/Counter 1 initialization
// Clock source: System Clock
// Clock value: Timer1 Stopped
// Mode: Normal top=0xFFFF
// OC1A output: Discon.
// OC1B output: Discon.
// Noise Canceler: Off
// Input Capture on Falling Edge
// Timer1 Overflow Interrupt: Off
// Input Capture Interrupt: Off
// Compare A Match Interrupt: Off
// Compare B Match Interrupt: Off
TCCR1A=0x00;
TCCR1B=0x00;
TCNT1H=0x00;
TCNT1L=0x00;
ICR1H=0x00;
ICR1L=0x00;
OCR1AH=0x00;
OCR1AL=0x00;
OCR1BH=0x00;
OCR1BL=0x00;

// Timer/Counter 2 initialization
// Clock source: System Clock
// Clock value: Timer2 Stopped
// Mode: Normal top=0xFF
// OC2 output: Disconnected
ASSR=0x00;
TCCR2=0x00;
TCNT2=0x00;
OCR2=0x00;

// External Interrupt(s) initialization
// INT0: Off
// INT1: Off
MCUCR=0x00;

// Timer(s)/Counter(s) Interrupt(s)
initialization
TIMSK=0x00;

// USART initialization
// Communication Parameters: 8 Data, 1
Stop, No Parity
// USART Receiver: Off
// USART Transmitter: On
// USART Mode: Asynchronous
// USART Baud Rate: 19200
UCSRA=0x00;
UCSRB=0x08;
UCSRC=0x86;
UBRRH=0x00;
UBRRL=0x33;;

// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by
Timer/Counter 1: Off
ACSR=0x80;
SFIOR=0x00;

// ADC initialization
// ADC Clock frequency: 1000.000 kHz
// ADC Voltage Reference: AREF pin
ADMUX=ADC_VREF_TYPE & 0xff;
ADCSRA=0x84;

// SPI initialization
// SPI disabled
SPCR=0x00;

// TWI initialization
// TWI disabled
TWCR=0x00;

while (1)
{
if(cnt1==50)   {
      proses1();    //sampling ADC0
      cnt1=0;   }
if(cnt2==250) {
      proses2();  //deteksi ada lagu
      cnt2=0;   }
if(cnt3==1000)      {
      proses3();    //deteksi ada mute
      cnt3=0;         }
```

```
if(cnt4==10)   {
      proses4();  //sampling ADC1 ADC2
      cnt4=0;   }
if(cnt5==50)   {
      proses5();    //deteksi gendang
      cnt5=0;   }
if(cnt6==1000)      {
      proses6();    //deteksi pola musik
      cnt6=0;          }
if(cnt7==25)   {
      proses7();    //Kirim data USART
      cnt7=0;   }
proses8();    //indikator LED
cnt1++;
cnt2++;
cnt3++;
cnt4++;
cnt5++;
cnt6++;
cnt7++;
delay_ms(1);
}
}
```

LAMPIRAN 4
DATASHEET

1. Datasheet ATmega8


ATmega8(L)

Features

- High-performance, Low-power Atmel®AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16MIPS Throughput at 16MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 8Kbytes of In-System Self-programmable Flash program memory
  - 512Bytes EEPROM
  - 1Kbyte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits In-System Programming by On-chip Boot Program True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Three PWM Channels
  - 8-channel ADC in TQFP and QFN/MLF package Eight Channels 10-bit Accuracy
  - 6-channel ADC in PDIP package Six Channels 10-bit Accuracy
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF
- Operating Voltages
  - 2.7V - 5.5V (ATmega8L)
  - 4.5V - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8MHz (ATmega8L)
  - 0 - 16MHz (ATmega8)
- Power Consumption at 4Mhz, 3V, 25°C
  - Active: 3.6mA
  - Idle Mode: 1.0mA
  - Power-down Mode: 0.5µA

8-bit Atmel with 8KBytes In-System Programmable Flash

ATmega8
ATmega8L

Rev.2486AA–AVR–02/2013

Pin Configurations

PDIP

TQFP Top View

MLF Top View

NOTE: The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the PCB to ensure good mechanical stability. If the center pad is left unconneted, the package might loosen from the PCB.

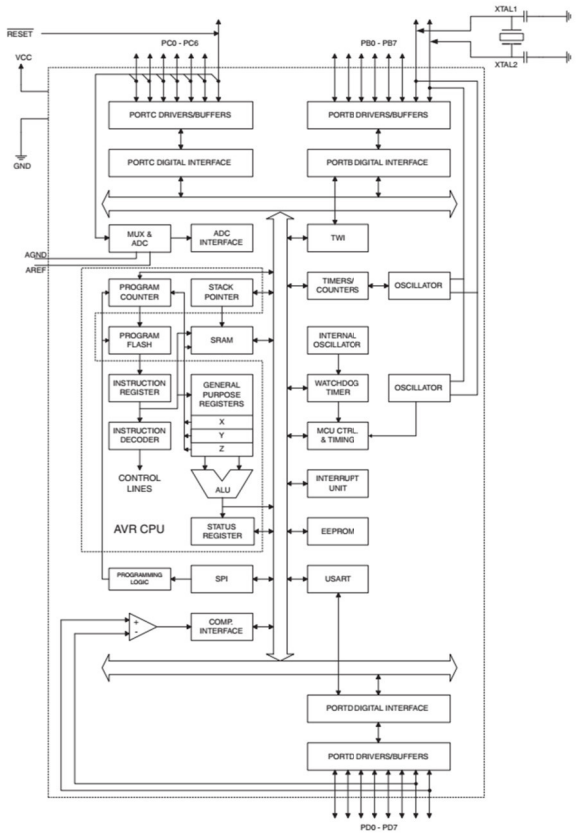
2486AA–AVR–02/2013 2

Overview

The Atmel®AVR® ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. Block Diagram



Pin Descriptions

VCC — Digital supply voltage.

GND — Ground.

Port B (PB7..PB0) XTAL1/XTAL2/TOSC1/ TOSC2 — Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in “Alternate Functions of Port B” on page 58 and “System Clock and Clock Options” on page 25.

Port C (PC5..PC0) — Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

PC6/$\overline{\text{RESET}}$ — If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated on page 61.

Port D (PD7..PD0) — Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8 as listed on page 63.

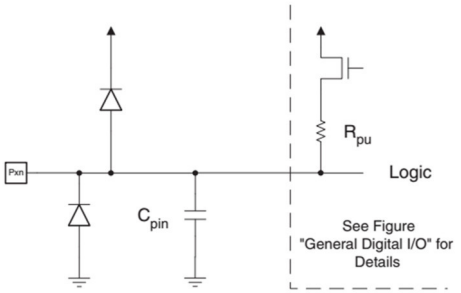
$\overline{\text{RESET}}$ — Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

I/O Ports

Introduction

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies when changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input). Each output buffer has symmetrical drive characteristics with both high sink and source capability. The pin driver is strong enough to drive LED displays directly. All port pins have individually selectable pull-up resistors with a supply-voltage invariant resistance. All I/O pins have protection diodes to both V_{CC} and Ground as indicated in Figure 21. Refer to "Electrical Characteristics – TA = -40°C to 85°C" on page 235 for a complete list of parameters.

Figure 21. I/O Pin Equivalent Schematic



All registers and bit references in this section are written in general form. A lower case "x" represents the numbering letter for the port, and a lower case "n" represents the bit number. However, when using the register or bit defines in a program, the precise form must be used (that is, PORTB3 for bit 3 in Port B, here documented generally as PORTxn). The physical I/O Registers and bit locations are listed in "Register Description for I/O Ports" on page 65.

Three I/O memory address locations are allocated for each port, one each for the Data Register – PORTx, Data Direction Register – DDRx, and the Port Input Pins – PINx. The Port Input Pins I/O location is read only, while the Data Register and the Data Direction Register are read/write. In addition, the Pull-up Disable – PUD bit in SFIOR disables the pull-up function for all pins in all ports when set.

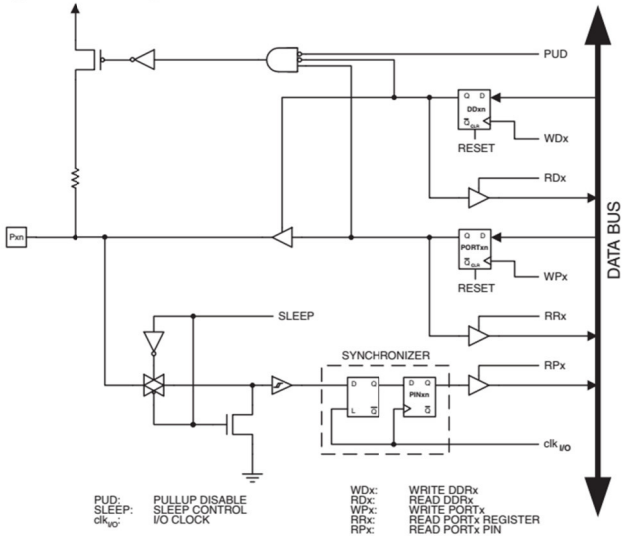
Using the I/O port as General Digital I/O is described in "Ports as General Digital I/O" . Most port pins are multiplexed with alternate functions for the peripheral features on the device. How each alternate function interferes with the port pin is described in "Alternate Port Functions" on page 56. Refer to the individual module sections for a full description of the alternate functions.

Note that enabling the alternate function of some of the port pins does not affect the use of the other pins in the port as general digital I/O.

Ports as General Digital I/O

The ports are bi-directional I/O ports with optional internal pull-ups. Figure 22 on page 52 shows a functional description of one I/O port pin, here generically called Pxn.

Figure 22. General Digital I/O(1)



Note: 1. WPx, WDx, RRx, RPx, and RDx are common to all pins within the same port. $clk_{I/O}$, SLEEP, and PUD are common to all ports

Configuring the Pin

Each port pin consists of 3 Register bits: DDxn, PORTxn, and PINxn. As shown in "Register Description for I/O Ports" on page 65, the DDxn bits are accessed at the DDRx I/O address, the PORTxn bits at the PORTx I/O address, and the PINxn bits at the PINx I/O address.

The DDxn bit in the DDRx Register selects the direction of this pin. If DDxn is written logic one, Pxn is configured as an output pin. If DDxn is written logic zero, Pxn is configured as an input pin.

If PORTxn is written logic one when the pin is configured as an input pin, the pull-up resistor is activated. To switch the pull-up resistor off, PORTxn has to be written logic zero or the pin has to be configured as an output pin. The port pins are tri-stated when a reset condition becomes active, even if no clocks are running.

If PORTxn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).

When switching between tri-state ({DDxn, PORTxn} = 0b00) and output high ({DDxn, PORTxn} = 0b11), an intermediate state with either pull-up enabled ({DDxn, PORTxn} = 0b01) or output low ({DDxn, PORTxn} = 0b10) must occur. Normally, the pull-up enabled state is fully acceptable, as a high-impedant environment will not notice the difference between a strong high driver and a pull-up. If this is not the case, the PUD bit in the SFIOR Register can be set to disable all pull-ups in all ports.

Switching between input with pull-up and output low generates the same problem. The user must use either the tri-state ({DDxn, PORTxn} = 0b00) or the output high state ({DDxn, PORTxn} = 0b11) as an intermediate step.

Table 20 summarizes the control signals for the pin value.

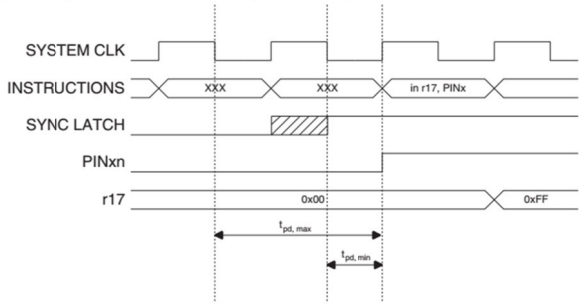
Table 20. Port Pin Configurations

DDxn	PORTxn	PUD (in SFIOR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if external pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

Reading the Pin Value

Independent of the setting of Data Direction bit DDxn, the port pin can be read through the PINxn Register Bit. As shown in Figure 22 on page 52, the PINxn Register bit and the preceding latch constitute a synchronizer. This is needed to avoid metastability if the physical pin changes value near the edge of the internal clock, but it also introduces a delay. Figure 23 shows a timing diagram of the synchronization when reading an externally applied pin value. The maximum and minimum propagation delays are denoted $t_{pd,max}$ and $t_{pd,min}$, respectively.

Figure 23. Synchronization when Reading an Externally Applied Pin Value



Consider the clock period starting shortly *after* the first falling edge of the system clock. The latch is closed when the clock is low, and goes transparent when the clock is high, as indicated by the shaded region of the "SYNC LATCH" signal. The signal value is latched when the system clock

USART

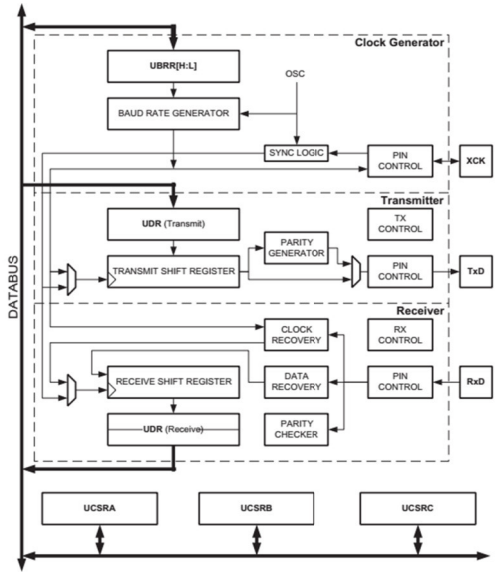
The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly-flexible serial communication device. The main features are:

- **Full Duplex Operation (Independent Serial Receive and Transmit Registers)**
- **Asynchronous or Synchronous Operation**
- **Master or Slave Clocked Synchronous Operation**
- **High Resolution Baud Rate Generator**
- **Supports Serial Frames with 5, 6, 7, 8, or 9 Databits and 1 or 2 Stop Bits**
- **Odd or Even Parity Generation and Parity Check Supported by Hardware**
- **Data OverRun Detection**
- **Framing Error Detection**
- **Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter**
- **Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**
- **Multi-processor Communication Mode**
- **Double Speed Asynchronous Communication Mode**

Overview

A simplified block diagram of the USART Transmitter is shown in Figure 61. CPU accessible I/O Registers and I/O pins are shown in bold.

Figure 61. USART Block Diagram(1)



Note: 1. Refer to "Pin Configurations" on page 2, Table 30 on page 64, and Table 29 on page 64 for USART pin placement

The dashed boxes in the block diagram separate the three main parts of the USART (listed from the top): Clock generator, Transmitter and Receiver. Control Registers are shared by all units. The clock generation logic consists of synchronization logic for external clock input used by synchronous slave operation, and the baud rate generator. The XCK (transfer clock) pin is only used by synchronous transfer mode. The Transmitter consists of a single write buffer, a serial Shift Register, Parity Generator and control logic for handling different serial frame formats. The write buffer allows a continuous transfer of data without any delay between frames. The Receiver is the most complex part of the USART module due to its clock and data recovery units. The recovery units are used for asynchronous data reception. In addition to the recovery units, the Receiver includes a parity checker, control logic, a Shift Register and a two level receive buffer (UDR). The Receiver supports the same frame formats as the Transmitter, and can detect Frame Error, Data OverRun and Parity Errors.

AVR USART vs. AVR UART – Compatibility

The USART is fully compatible with the AVR UART regarding:

- Bit locations inside all USART Registers
- Baud Rate Generation
- Transmitter Operation
- Transmit Buffer Functionality
- Receiver Operation

However, the receive buffering has two improvements that will affect the compatibility in some special cases:

- A second Buffer Register has been added. The two Buffer Registers operate as a circular FIFO buffer. Therefore the UDR must only be read once for each incoming data! More important is the fact that the Error Flags (FE and DOR) and the ninth data bit (RXB8) are buffered with the data in the receive buffer. Therefore the status bits must always be read before the UDR Register is read. Otherwise the error status will be lost since the buffer state is lost
- The Receiver Shift Register can now act as a third buffer level. This is done by allowing the received data to remain in the serial Shift Register (see Figure 61 on page 129) if the Buffer Registers are full, until a new start bit is detected. The USART is therefore more resistant to Data OverRun (DOR) error conditions

The following control bits have changed name, but have same functionality and register location:

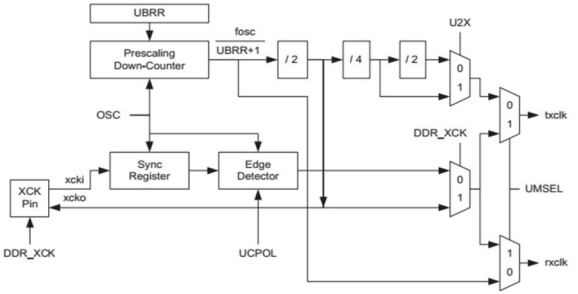
- CHR9 is changed to UCSZ2
- OR is changed to DOR

Clock Generation

The clock generation logic generates the base clock for the Transmitter and Receiver. The USART supports four modes of clock operation: normal asynchronous, double speed asynchronous, Master synchronous and Slave Synchronous mode. The UMSEL bit in USART Control and Status Register C (UCSRC) selects between asynchronous and synchronous operation. Double speed (Asynchronous mode only) is controlled by the U2X found in the UCSRA Register. When using Synchronous mode (UMSEL = 1), the Data Direction Register for the XCK pin (DDR_XCK) controls whether the clock source is internal (Master mode) or external (Slave mode). The XCK pin is only active when using Synchronous mode.

Figure 62 on page 131 shows a block diagram of the clock generation logic.

Figure 62. Clock Generation Logic, Block Diagram



Signal description:

txclk	Transmitter clock. (Internal Signal)
rxclk	Receiver base clock. (Internal Signal)
xcki	Input from XCK pin (internal Signal). Used for synchronous slave operation
xcko	Clock output to XCK pin (Internal Signal). Used for synchronous master operation
fosc	XTAL pin frequency (System Clock)

Internal Clock Generation – The Baud Rate Generator

Internal clock generation is used for the asynchronous and the Synchronous Master modes of operation. The description in this section refers to Figure 62.

The USART Baud Rate Register (UBRR) and the down-counter connected to it function as a programmable prescaler or baud rate generator. The down-counter, running at system clock (fosc), is loaded with the UBRR value each time the counter has counted down to zero or when the UBRRL Register is written. A clock is generated each time the counter reaches zero. This clock is the baud rate generator clock output (= fosc/(UBRR+1)). The Transmitter divides the baud rate generator clock output by 2, 8, or 16 depending on mode. The baud rate generator output is used directly by the Receiver's clock and data recovery units. However, the recovery units use a state machine that uses 2, 8, or 16 states depending on mode set by the state of the UMSEL, U2X and DDR_XCK bits.

Table 52 on page 132 contains equations for calculating the baud rate (in bits per second) and for calculating the UBRR value for each mode of operation using an internally generated clock source.

Examples of Baud Rate Setting

For standard crystal and resonator frequencies, the most commonly used baud rates for asynchronous operation can be generated by using the UBRR settings in Table 60. UBRR values which yield an actual baud rate differing less than 0.5% from the target baud rate, are bold in the table. Higher error ratings are acceptable, but the Receiver will have less noise resistance when the error ratings are high, especially for large serial frames (see "Asynchronous Operational Range" on page 144). The error values are calculated using the following equation:

$$\text{Error}[\%] = \left(\frac{\text{BaudRate}_{\text{Closest Match}}}{\text{BaudRate}} - 1\right) \bullet 100\%$$

Table 60. Examples of UBRR Settings for Commonly Used Oscillator Frequencies

Baud Rate (bps)	f_{osc} = 1.0000MHz				f_{osc} = 1.8432MHz				f_{osc} = 2.0000MHz			
	U2X = 0		U2X = 1		U2X = 0		U2X = 1		U2X = 0		U2X = 1	
	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error
2400	**25**	**0.2%**	**51**	**0.2%**	**47**	**0.0%**	**95**	**0.0%**	**51**	**0.2%**	**103**	**0.2%**
4800	**12**	**0.2%**	**25**	**0.2%**	**23**	**0.0%**	**47**	**0.0%**	**25**	**0.2%**	**51**	**0.2%**
9600	6	-7.0%	**12**	**0.2%**	**11**	**0.0%**	**23**	**0.0%**	**12**	**0.2%**	**25**	**0.2%**
14.4k	3	8.5%	8	-3.5%	**7**	**0.0%**	**15**	**0.0%**	8	-3.5%	16	2.1%
19.2k	2	8.5%	6	-7.0%	**5**	**0.0%**	**11**	**0.0%**	6	-7.0%	**12**	**0.2%**
28.8k	1	8.5%	3	8.5%	**3**	**0.0%**	**7**	**0.0%**	3	8.5%	8	-3.5%
38.4k	1	-18.6%	2	8.5%	**2**	**0.0%**	**5**	**0.0%**	2	8.5%	6	-7.0%
57.6k	0	8.5%	1	8.5%	**1**	**0.0%**	**3**	**0.0%**	1	8.5%	3	8.5%
76.8k	–	–	1	-18.6%	1	-25.0%	**2**	**0.0%**	1	-18.6%	2	8.5%
115.2k	–	–	0	8.5%	**0**	**0.0%**	**1**	**0.0%**	0	8.5%	1	8.5%
230.4k	–	–	–	–	–	–	**0**	**0.0%**	–	-	–	–
250k	–	–	–	–	–	–	–	–	–	–	**0**	**0.0%**
Max [1]	62.5kbps		125kbps		115.2kbps		230.4kbps		125kbps		250kbps	

1. UBRR = 0, Error = 0.0%

Analog-to-Digital Converter

Features

- **10-bit Resolution**
- **0.5 LSB Integral Non-linearity**
- **±2 LSB Absolute Accuracy**
- **13µs - 260µs Conversion Time**
- **Up to 15 kSPS at Maximum Resolution**
- **6 Multiplexed Single Ended Input Channels**
- **2 Additional Multiplexed Single Ended Input Channels (TQFP and QFN/MLF Package only)**
- **Optional Left Adjustment for ADC Result Readout**
- **0 - V_{CC} ADC Input Voltage Range**
- **Selectable 2.56V ADC Reference Voltage**
- **Free Running or Single Conversion Mode**
- **Interrupt on ADC Conversion Complete**
- **Sleep Mode Noise Canceler**

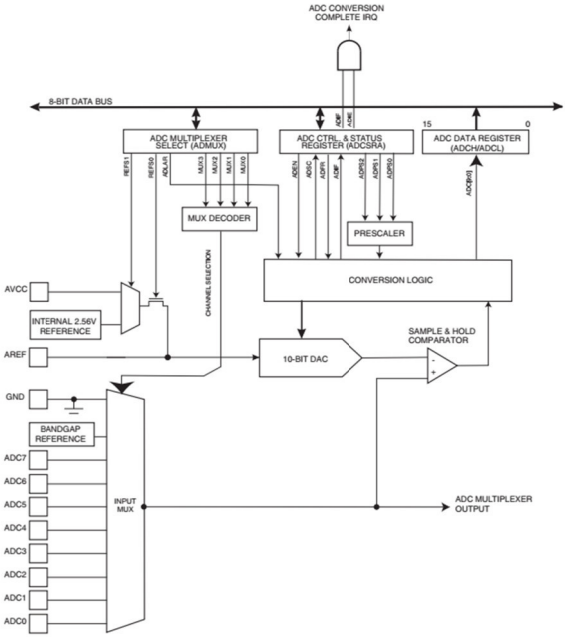
The ATmega8 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer which allows eight single-ended voltage inputs constructed from the pins of Port C. The single-ended voltage inputs refer to 0V (GND).

The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 90 on page 190.

The ADC has a separate analog supply voltage pin, AV_{CC}. AV_{CC} must not differ more than ±0.3V from V_{CC}. See the paragraph "ADC Noise Canceler" on page 195 on how to connect this pin.

Internal reference voltages of nominally 2.56V or AV_{CC} are provided On-chip. The voltage reference may be externally decoupled at the AREF pin by a capacitor for better noise performance.

Figure 90. Analog to Digital Converter Block Schematic Operation



The ADC converts an analog input voltage to a 10-bit digital value through successive approximation. The minimum value represents GND and the maximum value represents the voltage on the AREF pin minus 1 LSB. Optionally, AV_{CC} or an internal 2.56V reference voltage may be connected to the AREF pin by writing to the REFSn bits in the ADMUX Register. The internal voltage reference may thus be decoupled by an external capacitor at the AREF pin to improve noise immunity.

The analog input channel is selected by writing to the MUX bits in ADMUX. Any of the ADC input pins, as well as GND and a fixed bandgap voltage reference, can be selected as single ended inputs to the ADC. The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSRA. Voltage reference and input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power saving sleep modes.

The ADC generates a 10-bit result which is presented in the ADC Data Registers, ADCH and ADCL. By default, the result is presented right adjusted, but can optionally be presented left adjusted by setting the ADLAR bit in ADMUX.

If the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH, to ensure that the content of the Data Registers belongs to the same conversion. Once ADCL is read, ADC access to Data Registers is blocked. This means that if ADCL has been read, and a conversion completes before ADCH is read, neither register is updated and the result from the conversion is lost. When ADCH is read, ADC access to the ADCH and ADCL Registers is re-enabled.

The ADC has its own interrupt which can be triggered when a conversion completes. When ADC access to the Data Registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result is lost.

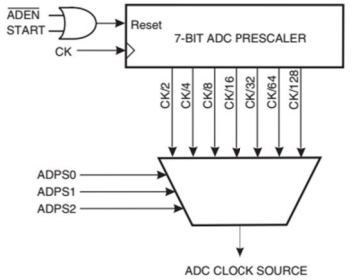
Starting a Conversion

A single conversion is started by writing a logical one to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be cleared by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

In Free Running mode, the ADC is constantly sampling and updating the ADC Data Register. Free Running mode is selected by writing the ADFR bit in ADCSRA to one. The first conversion must be started by writing a logical one to the ADSC bit in ADCSRA. In this mode the ADC will perform successive conversions independently of whether the ADC Interrupt Flag, ADIF is cleared or not.

Prescaling and Conversion Timing

Figure 91. ADC Prescaler



By default, the successive approximation circuitry requires an input clock frequency between 50kHz and 200kHz to get maximum resolution. If a lower resolution than 10 bits is needed, the input clock frequency to the ADC can be higher than 200kHz to get a higher sample rate.

The ADC module contains a prescaler, which generates an acceptable ADC clock frequency from any CPU frequency above 100kHz. The prescaling is set by the ADPS bits in ADCSRA. The prescaler starts counting from the moment the ADC is switched on by setting the ADEN bit in ADCSRA. The prescaler keeps running for as long as the ADEN bit is set, and is continuously reset when ADEN is low.

When initiating a single ended conversion by setting the ADSC bit in ADCSRA, the conversion starts at the following rising edge of the ADC clock cycle. A normal conversion takes 13 ADC clock cycles. The first conversion after the ADC is switched on (ADEN in ADCSRA is set) takes 25 ADC clock cycles in order to initialize the analog circuitry.

The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of an first conversion. When a conversion is complete, the result is written to the ADC Data Registers, and ADIF is set. In single conversion mode, ADSC is cleared simultaneously. The software may then set ADSC again, and a new conversion will be initiated on the first rising ADC clock edge.

In Free Running mode, a new conversion will be started immediately after the conversion completes, while ADSC remains high. For a summary of conversion times, see Table 73 on page 193.

Figure 92. ADC Timing Diagram, First Conversion (Single Conversion Mode)

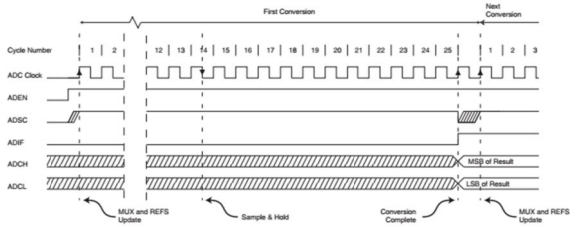


Figure 93. ADC Timing Diagram, Single Conversion

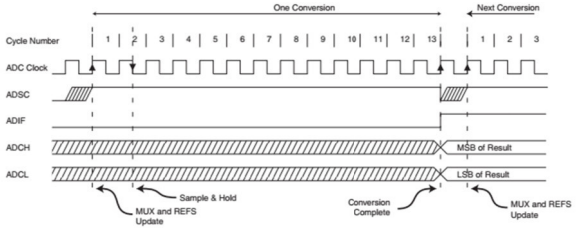


Figure 94. ADC Timing Diagram, Free Running Conversion

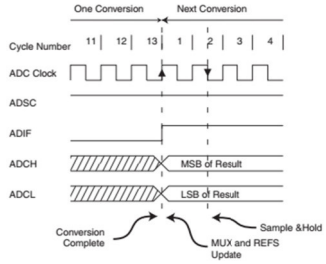


Table 73. ADC Conversion Time

Condition	Sample & Hold (Cycles from Start of Conversion)	Conversion Time (Cycles)
Extended conversion	13.5	25
Normal conversions, single ended	1.5	13

Changing Channel or Reference Selection

The MUXn and REFS1:0 bits in the ADMUX Register are single buffered through a temporary register to which the CPU has random access. This ensures that the channels and reference selection only takes place at a safe point during the conversion. The channel and reference selection is continuously updated until a conversion is started. Once the conversion starts, the channel and reference selection is locked to ensure a sufficient sampling time for the ADC. Continuous updating resumes in the last ADC clock cycle before the conversion completes (ADIF in ADCSRA is set). Note that the conversion starts on the following rising ADC clock edge after ADSC is written. The user is thus advised not to write new channel or reference selection values to ADMUX until one ADC clock cycle after ADSC is written.

If both ADFR and ADEN is written to one, an interrupt event can occur at any time. If the ADMUX Register is changed in this period, the user cannot tell if the next conversion is based on the old or the new settings. ADMUX can be safely updated in the following ways:

1. When ADFR or ADEN is cleared
2. During conversion, minimum one ADC clock cycle after the trigger event
3. After a conversion, before the Interrupt Flag used as trigger source is cleared

When updating ADMUX in one of these conditions, the new settings will affect the next ADC conversion.

ADC Input Channels

When changing channel selections, the user should observe the following guidelines to ensure that the correct channel is selected:

In Single Conversion mode, always select the channel before starting the conversion. The channel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the conversion to complete before changing the channel selection.

In Free Running mode, always select the channel before starting the first conversion. The channel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the first conversion to complete, and then change the channel selection. Since the next conversion has already started automatically, the next result will reflect the previous channel selection. Subsequent conversions will reflect the new channel selection.

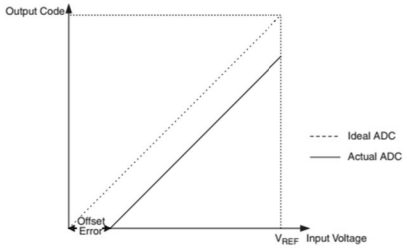
ADC Voltage Reference

The reference voltage for the ADC (V_{REF}) indicates the conversion range for the ADC. Single ended channels that exceed V_{REF} will result in codes close to 0x3FF. V_{REF} can be selected as either AV_{CC}, internal 2.56V reference, or external AREF pin.

AV_{CC} is connected to the ADC through a passive switch. The internal 2.56V reference is generated from the internal bandgap reference (V_{BG}) through an internal amplifier. In either case, the external AREF pin is directly connected to the ADC, and the reference voltage can be made more immune to noise by connecting a capacitor between the AREF pin and ground. V_{REF} can also be measured at the AREF pin with a high impedant voltmeter. Note that V_{REF} is a high impedant source, and only a capacitive load should be connected in a system.

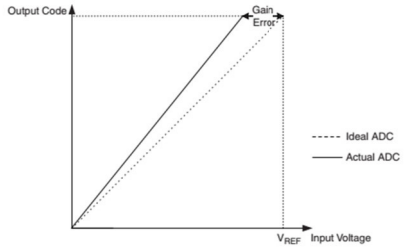
If the user has a fixed voltage source connected to the AREF pin, the user may not use the other reference voltage options in the application, as they will be shorted to the external voltage. If no external voltage is applied to the AREF pin, the user may switch between AV_{CC} and 2.56V as reference selection. The first ADC conversion result after switching reference voltage source may be inaccurate, and the user is advised to discard this result.

Figure 97. Offset Error



- Gain error: After adjusting for offset, the gain error is found as the deviation of the last transition (0x3FE to 0x3FF) compared to the ideal transition (at 1.5 LSB below maximum). Ideal value: 0 LSB

Figure 98. Gain Error



ADC Conversion Result

After the conversion is complete (ADIF is high), the conversion result can be found in the ADC Result Registers (ADCL, ADCH).

For single ended conversion, the result is:

$$ADC = \frac{V_{IN} \cdot 1024}{V_{REF}}$$

where V_{IN} is the voltage on the selected input pin and V_{REF} the selected voltage reference (see Table 74 and Table 75). 0x000 represents ground, and 0x3FF represents the selected reference voltage minus one LSB.

ADC Multiplexer Selection Register – ADMUX

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7:6 – REFS1:0: Reference Selection Bits**

These bits select the voltage reference for the ADC, as shown in Table 74. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set). The internal voltage reference options may not be used if an external reference voltage is being applied to the AREF pin.

Table 74. Voltage Reference Selections for ADC

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, Internal V_{ref} turned off
0	1	AV_{CC} with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

- **Bit 5 – ADLAR: ADC Left Adjust Result**

The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit will affect the ADC Data Register immediately, regardless of any ongoing conversions. For a complete description of this bit, see "The ADC Data Register – ADCL and ADCH" on page 201.

- **Bits 3:0 – MUX3:0: Analog Channel Selection Bits**

The value of these bits selects which analog inputs are connected to the ADC. See Table 75 for details. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set).

Table 75. Input Channel Selections

MUX3..0	Single Ended Input
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5

Table 75. Input Channel Selections (Continued)

MUX3..0	Single Ended Input
0110	ADC6
0111	ADC7
1000	
1001	
1010	
1011	
1100	
1101	
1110	1.30V (V_{BG})
1111	0V (GND)

ADC Control and Status Register A – ADCSRA

Bit	7	6	5	4	3	2	1	0	
	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ADEN: ADC Enable**

Writing this bit to one enables the ADC. By writing it to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress, will terminate this conversion.

- **Bit 6 – ADSC: ADC Start Conversion**

In Single Conversion mode, write this bit to one to start each conversion. In Free Running mode, write this bit to one to start the first conversion. The first conversion after ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, will take 25 ADC clock cycles instead of the normal 13. This first conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. Writing zero to this bit has no effect.

- **Bit 5 – ADFR: ADC Free Running Select**

When this bit is set (one) the ADC operates in Free Running mode. In this mode, the ADC samples and updates the Data Registers continuously. Clearing this bit (zero) will terminate Free Running mode.

- **Bit 4 – ADIF: ADC Interrupt Flag**

This bit is set when an ADC conversion completes and the Data Registers are updated. The ADC Conversion Complete Interrupt is executed if the ADIE bit and the I-bit in SREG are set. ADIF is cleared by hardware when executing the corresponding interrupt Handling Vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a Read-Modify-Write on ADCSRA, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- **Bit 3 – ADIE: ADC Interrupt Enable**

When this bit is written to one and the I-bit in SREG is set, the ADC Conversion Complete Interrupt is activated.

LM358, LM258, LM158, LM2904 Dual Operational Amplifiers

1 Features

- Wide Supply Ranges
  - Single Supply: 3 V to 32 V (26 V for LM2904)
  - Dual Supplies: ±1.5 V to ±16 V (±13 V for LM2904)
- Low Supply-Current Drain, Independent of Supply Voltage: 0.7 mA Typical
- Wide Unity Gain Bandwidth: 0.7 MHz
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
  - Input Offset Voltage: 3 mV Typical A Versions: 2 mV Typical
  - Input Offset Current: 2 nA Typical
  - Input Bias Current: 20 nA Typical A Versions: 15 nA Typical
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: 32 V (26 V for LM2904)
- Open-Loop Differential Voltage Gain: 100 dB Typical
- Internal Frequency Compensation
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- DVD Recorder and Players
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using Modbus
- Weigh Scales

3 Description

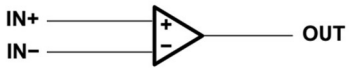
These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply or split supply over a wide range of voltages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMx58, LMx58x, LM2904, LM2904V	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SO (8)	5.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	PDIP (8)	9.81 mm × 6.35 mm
LMx58, LMx58x, LM2904V	CDIP (8)	9.60 mm × 6.67 mm
	LCCC (20)	8.89 mm × 8.89 mm

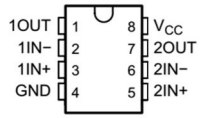
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Amplifier)

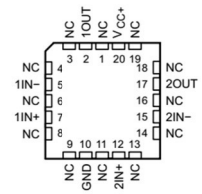


5 Pin Configuration and Functions

D, DGK, P, PS, PW and JG Package
8-Pin SOIC, VSSOP, PDIP, SO, TSSOP and CDIP
(Top View)



FK Package
20-Pin LCCC
(Top View)



NC - No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	LCCC NO.	SOIC, SSOP, CDIP, PDIP SO, TSSOP, CFP NO.		
1IN–	5	2	I	Negative input
1IN+	7	3	I	Positive input
1OUT	2	1	O	Output
2IN–	15	6	I	Negative input
2IN+	12	5	I	Positive input
2OUT	17	7	O	Output
GND	10	4	—	Ground
NC	1	—	—	Do not connect
	3			
	4			
	6			
	8			
	9			
	11			
	13			
	14			
	16			
	18			
	19			
V_{CC}	—	8	—	Power supply
V_{CC+}	20	—	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				LMx58, LMx58x, LM2904V		LM2904		UNIT
				MIN	MAX	MIN	MAX	
V_{CC}		Supply voltage(2)		–0.3	±16 or 32	–0.3	±13 or 26	V
V_{ID}		Differential input voltage(3)		–32	32	–26	26	V
V_I	either input	Input voltage		–0.3	32	–0.3	26	V
		Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, V_{CC} ≤ 15 V(4)			Unlimited		Unlimited	s
T_A		Operating free air temperature	LM158, LM158A	–55	125			°C
			LM258, LM258A	–25	85			
			LM358, LM358A	0	70			
			LM2904	–40	125	–40	125	
T_J		Operating virtual junction temperature			150		150	°C
		Case temperature for 60 seconds	FK package		260			°C
		Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	JG package		300		300	°C
T_{stg}		Storage temperature		–65	150	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+, with respect to IN−.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			LMx58, LMx58x, LM2904V		LM2904		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	30	3	26	V
V_{CM}	Common-mode voltage		0	V_{CC} – 2	0	V_{CC} – 2	V
T_A	Operating free air temperature	LM158	–55	125			°C
		LM2904	–40	125	–40	125	
		LM358	0	70			
		LM258	–25	85			

6.4 Thermal Information

THERMAL METRIC(1)		LMx58, LMx58x, LM2904V, LM2904					LMx58, LMx58x, LM2904 V	LMx58, LMx58x, LM2904 V	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	FK (LCCC)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	172	85	95	149	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.2	—	—	—	—	5.61	14.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for LMx58

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		T_A(2)	LM158 LM258			LM358			UNIT
					MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = $V_{ICR(min)}$, V_O = 1.4 V		25°C		3	5		3	7	mV
				Full range			7			9	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		7			7		µV/°C
I_{IO}	Input offset current	V_O = 1.4 V		25°C		2	30		2	50	nA
				Full range			100			150	
α_{IIO}	Average temperature coefficient of input offset current			Full range		10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–20	–150		–20	–250	nA
				Full range			–300			–500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX		25°C	0 to V_{CC} – 1.5			0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			0 to V_{CC} – 2			
V_{OH}	High-level output voltage	R_L ≥ 2 kΩ		25°C	V_{CC} – 1.5			V_{CC} – 1.5			V
		R_L ≥ 10 kΩ		25°C							
		V_{CC} = MAX	R_L = 2 kΩ	Full range	26			26			
			R_L ≥ 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ		Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ		25°C	50	100		25	100		V/mV
				Full range	25			15			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to MAX, V_{IC} = $V_{ICR(min)}$		25°C	70	80		65	80		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC} /ΔV_{IO})	V_{CC} = 5 V to MAX		25°C	65	100		65	100		dB
V_{O1}/ V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	Source	25°C	–20	–30		–20	–30		mA
				Full range	–10			–10			
		V_{CC} = 15 V, V_{ID} = –1 V, V_O = 15 V	Sink	25°C	10	20		10	20		
				Full range	5			5			
		V_{ID} = –1 V, V_O = 200 mV		25°C	12	30		12	30		µA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at –5 V, V_O = 0		25°C		±40	±60		±40	±60	mA

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 26 V for LM2902 and 30 V for the others.
(2) Full range is –55°C to 125°C for LM158, –25°C to 85°C for LM258, and 0°C to 70°C for LM358, and –40°C to 125°C for LM2904.
(3) All typical values are at T_A = 25°C

6.10 Typical Characteristics

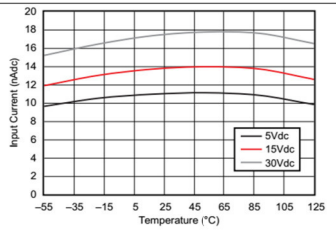


Figure 1. Input Current vs. Temperature

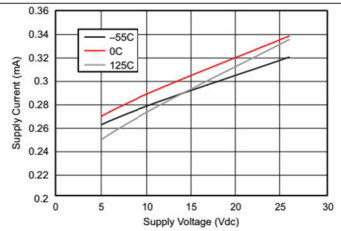


Figure 2. Supply Current vs. Supply Voltage

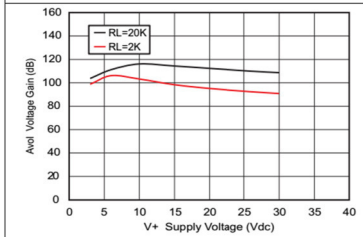


Figure 3. Voltage Gain vs. Supply Voltage

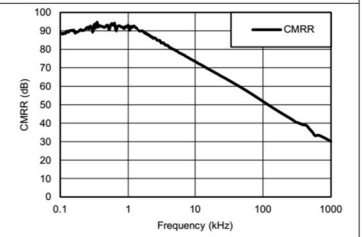


Figure 4. Common-mode Rejection Ratio vs. Frequency

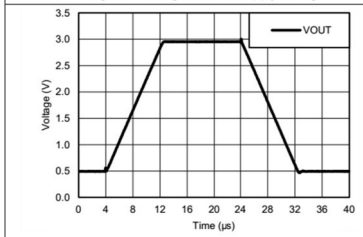


Figure 5. Voltage Follower Large Signal Response (50 pF)

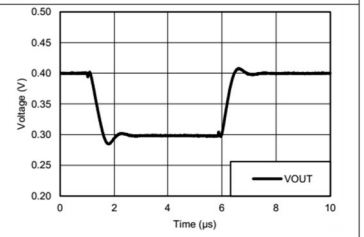


Figure 6. Voltage Follower Small Signal Response (50 pF)

Typical Characteristics (continued)

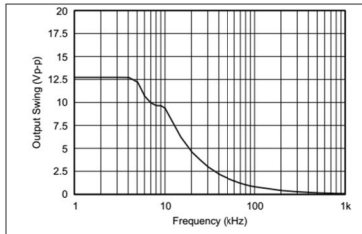


Figure 7. Maximum Output Swing vs. Frequency (V_{CC} = 15 V)

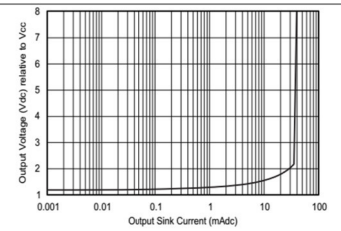


Figure 8. Output Sourcing Characteristics

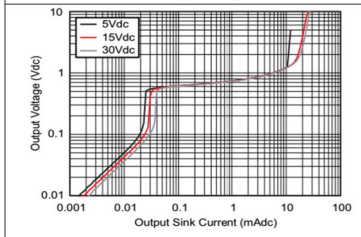


Figure 9. Output Sinking Characteristics

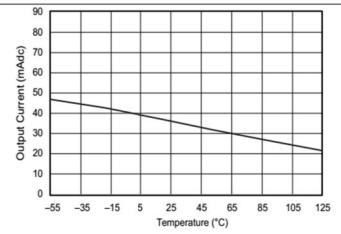


Figure 10. Source Current Limiting

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CP2102/9

SINGLE-CHIP USB-TO-UART BRIDGE

For newer designs, the CP2102N devices offer compatible footprints and are recommended for use instead of the CP2102/9. See the Silicon Labs website (www.silabs.com/usbxpress) for more information.

Single-Chip USB to UART Data Transfer
- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- Internal 1024-byte programmable ROM for vendor ID, product ID, serial number, power descriptor, release number, and product description strings
  - EEPROM (CP2102)
  - EPROM (One-time programmable) (CP2109)
- On-chip power-on reset circuit
- On-chip voltage regulator
  - 3.3 V output (CP2102)
  - 3.45 V output (CP2109)
- 100% pin and software compatible with CP2101

USB Function Controller
- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB suspend states supported via SUSPEND pins

Asynchronous Serial Data BUS (UART)
- All handshaking and modem interface signals
- Data formats supported:
  - Data bits: 5, 6, 7, and 8
  - Stop bits: 1, 1.5, and 2
  - Parity: odd, even, mark, space, no parity
- Baud rates: 300 bps to 1 Mbps
- 576 Byte receive buffer; 640 byte transmit buffer
- Hardware or X-On/X-Off handshaking supported
- Event character support
- Line break transmission

Virtual COM Port Device Drivers
- Works with existing COM port PC Applications
- Royalty-free distribution license
- Windows 8/7/Vista/Server 2003/XP/2000
- Mac OS-X/OS-9
- Linux

USBXpress™ Direct Driver Support
- Royalty-Free Distribution License
- Windows 7/Vista/XP/Server 2003/2000
- Windows CE

Example Applications
- Upgrade of RS-232 legacy devices to USB
- Cellular phone USB interface cable
- USB interface cable
- USB to RS-232 serial adapter

Supply Voltage
- Self-powered: 3.0 to 3.6 V
- USB bus powered: 4.0 to 5.25 V

Package
- RoHS-compliant 28-pin QFN (5x5 mm)

Ordering Part Numbers
- CP2102-GM
- CP2109-A01-GM

Temperature Range: –40 to +85 °C

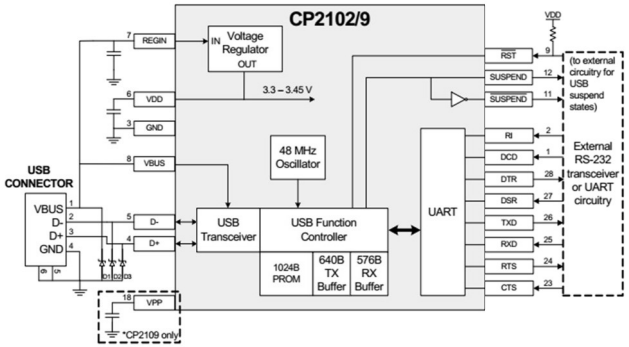

Figure 1. Example System Diagram

3. Electrical Specifications

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature under Bias	T_{BIAS}		–55	—	125	°C
Storage Temperature	T_{STG}		–65	—	150	°C
Voltage on V_{DD} with respect to GND	V_{DD}		–0.3	—	4.2	V
Maximum Total Current through V_{DD} and GND			—	—	500	mA
Maximum Output Current sunk by $\overline{RST}$ or any I/O pin			—	—	100	mA
CP2102						
Voltage on any I/O Pin, VBUS, or $\overline{RST}$ with respect to GND			–0.3	—	5.8	V
CP2109						
Voltage on any I/O Pin, VBUS, or $\overline{RST}$ with respect to GND		$V_{DD} \geq 3.0$ V V_{DD} not powered	–0.3 –0.3	— —	5.8 V_{DD} + 3.6	V

Note: Stresses above those listed may cause permanent device damage. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Table 3. Recommended Operating Conditions
V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Supply Current - USB Pull-up[1]	I_{PU}		—	200	230	µA
Specified Operating Temperature Range	T_A		–40	—	+85	°C
Thermal Resistance[2]	θ_{JA}		—	32	—	°C/W
CP2102						
Supply Current—Normal[3]	I_{REGIN}	Normal Operation; V_{REG} Enabled	—	20	26	mA
Supply Current—Suspended[3]		Bus Powered; V_{REG} Enabled	—	80	100	µA
CP2109						
Supply Current—Normal[3]	I_{REGIN}	Normal Operation; V_{REG} Enabled	—	17	23	mA
Supply Current—Suspended[3]		Bus Powered; V_{REG} Enabled	—	90	230	µA

Notes:
1. The USB Pull-up supply current values are calculated values based on USB specifications. USB Pull-up supply current is current flowing from V_{DD} to GND through USB pull-down/pull-up resistors on D+ and D-.
2. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.
3. USB Pull-up current should be added for total supply current. Normal and suspended supply current is current flowing into V_{REGIN}. Normal and suspended supply current is guaranteed by characterization.

Table 4. UART and Suspend I/O DC Electrical Characteristics
V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Baud Rate			—	—	921600	bps
Input Leakage Current	I_L		—	25	50	µA
CP2102						
Output High Voltage	V_{OH}	I_{OH} = –10 µA I_{OH} = –3 mA I_{OH} = –10 mA	V_{DD} – 0.1 V_{DD} – 0.7 —	— — V_{DD} – 0.8	— — —	V
Output Low Voltage	V_{OL}	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA	— — —	— — 1.0	0.1 0.6 —	V
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
CP2109						
Output High Voltage	V_{OH}	I_{OH} = –10 µA I_{OH} = –3 mA I_{OH} = –10 mA	V_{DD} – 0.1 V_{DD} – 0.2 —	— — V_{DD} – 0.4	— — —	V
Output Low Voltage	V_{OL}	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA	— — —	— — 0.6	0.1 0.4 —	V
Input High Voltage	V_{IH}		0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V

Table 5. Reset Electrical Characteristics
–40 to +85 °C unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} Ramp Time	t_{RMP}	Time to V_{DD} ≥ 2.7 V	—	—	1	ms
$\overline{RST}$ Low Time to Generate a System Reset	t_{RSTL}		15	—	—	µs
CP2102						
$\overline{RST}$ Input High Voltage	$V_{IHRESET}$		0.7 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage	$V_{ILRESET}$		—	—	0.25 x V_{DD}	V
CP2109						
$\overline{RST}$ Input High Voltage	$V_{IHRESET}$		0.75 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage	$V_{ILRESET}$		—	—	0.6	V

4. Pinout and Package Definitions

Table 9. CP2102/9 Pin Definitions

Name	Pin #	Type	Description
V_{DD}	6	Power In Power Out	3.0–3.6 V Power Supply Voltage Input. 3.3 V Voltage Regulator Output. See "10. Voltage Regulator" on page 19.
GND	3		Ground
RST	9	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs.
REGIN	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
NC[1] / V_{PP}[2]	18	 A Power	This pin should be left unconnected or tied to V_{DD}. This pin is unused on the CP2102 and may be connected to the Vpp programming capacitor to maintain board compatibility with the CP2109. V_{PP} Programming Supply Voltage
D+	4	D I/O	USB D+
D–	5	D I/O	USB D–
TXD	26	D Out	Asynchronous data output (UART Transmit)
RXD	25	D In	Asynchronous data input (UART Receive)
CTS	23[3]	D In	Clear To Send control input (active low)
RTS	24[3]	D Out	Ready to Send control output (active low)
DSR	27[3]	D in	Data Set Ready control input (active low)
DTR	28[3]	D Out	Data Terminal Ready control output (active low)
DCD	1[3]	D In	Data Carrier Detect control input (active low)
RI	2[3]	D In	Ring Indicator control input (active low)
SUSPEND	12[3]	D Out	This pin is driven high when the CP2102/9 enters the USB suspend state.
$\overline{\text{SUSPEND}}$	11[3]	D Out	This pin is driven low when the CP2102/9 enters the USB suspend state.
NC	10, 13–22		These pins should be left unconnected or tied to V_{DD}.

Notes:
1. For CP2102, pin is no connect (NC).
2. For CP2109, pin is V_{PP}. V_{PP} can be left unconnected when not used for in-application programming.
3. Pins can be left unconnected when not used.

7. Asynchronous Serial Data Bus (UART) Interface

The CP2102/9 UART interface consists of the TX (transmit) and RX (receive) data signals as well as the RTS, CTS, DSR, DTR, DCD, and RI control signals. The UART supports RTS/CTS, DSR/DTR, and X-On/X-Off handshaking.

The UART is programmable to support a variety of data formats and baud rates. If the Virtual COM Port drivers are used, the data format and baud rate are set during COM port configuration on the PC. If the USBXpress drivers are used, the CP2102/9 is configured through the USBXpress API. The data formats and baud rates available are listed in Table 12.

Table 12. Data Formats and Baud Rates

Data Bits	5, 6, 7, and 8
Stop Bits	1, 1.5[1], and 2
Parity Type	None, Even, Odd, Mark, Space
Baud Rates[2]	300, 600, 1200, 1800, 2400, 4000, 4800, 7200, 9600, 14400, 16000, 19200, 28800, 38400, 51200, 56000, 57600, 64000, 76800, 115200, 128000, 153600, 230400, 250000, 256000, 460800, 500000, 576000, 921600[3]

Notes:
1. 5-bit only.
2. Additional baud rates are supported. See “AN721: CP210x/CP211x Device Customization Guide”.
3. 7 or 8 data bits only.