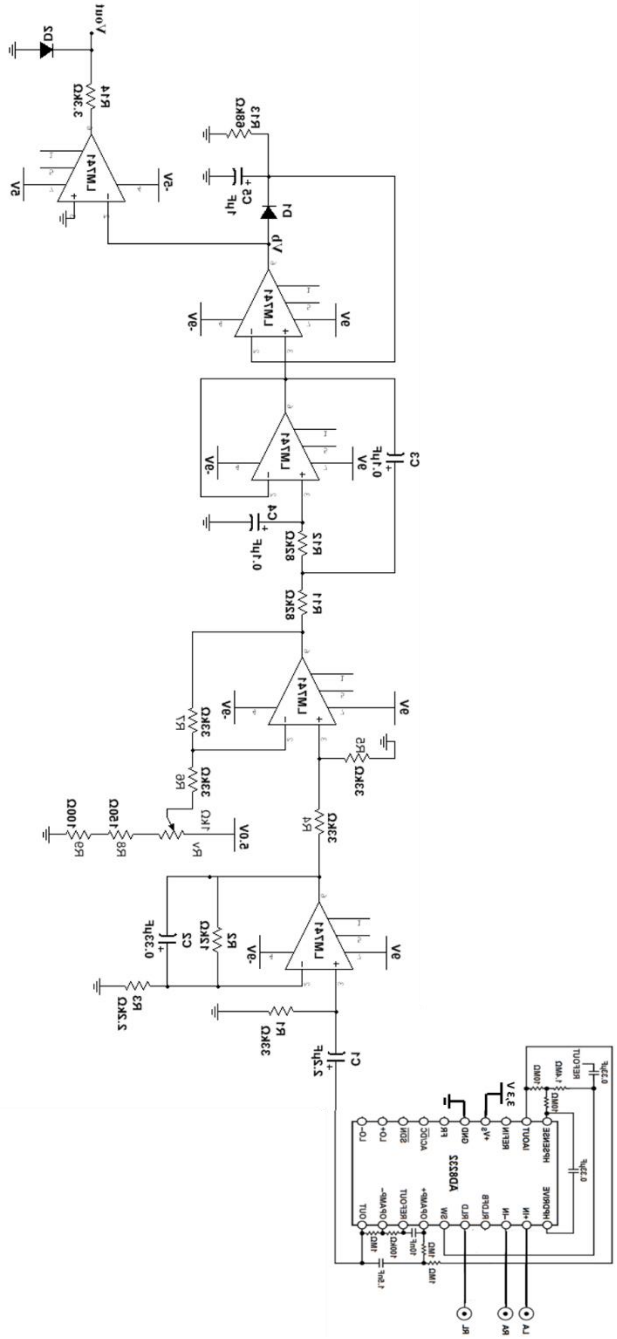
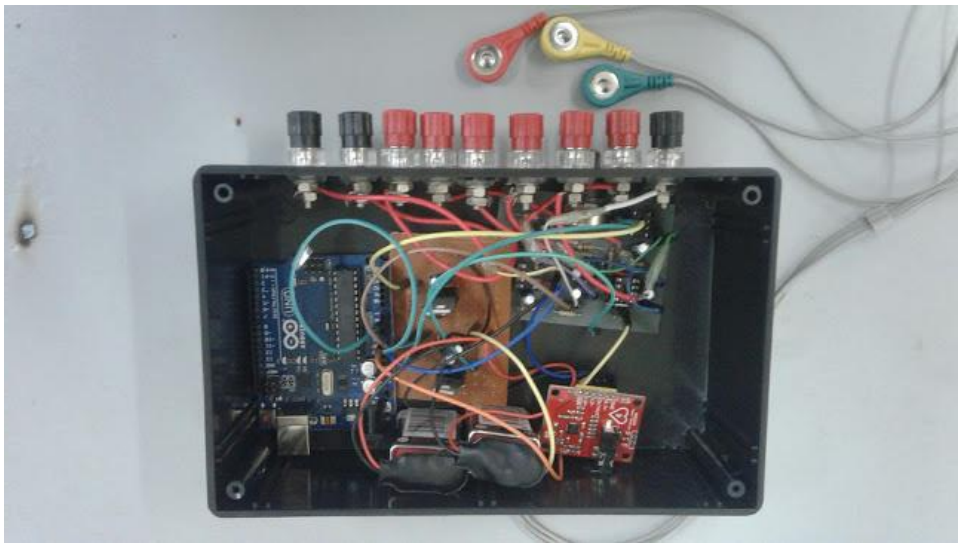
LAMPIRAN

1. Skematik sistem



2. Dokumentasi Alat



Single-Lead, Heart Rate Monitor Front End

Data Sheet **AD8232**

FEATURES

- Fully integrated single-lead ECG front end
- Low supply current: 170 µA (typical)
- Common-mode rejection ratio: 80 dB (dc to 60 Hz)
- Two or three electrode configurations
- High signal gain (G = 100) with dc blocking capabilities
- 2-pole adjustable high-pass filter
- Accepts up to ±300 mV of half cell potential
- Fast restore feature improves filter settling
- Uncommitted op amp
- 3-pole adjustable low-pass filter with adjustable gain
- Leads off detection: ac or dc options
- Integrated right leg drive (RLD) amplifier
- Single-supply operation: 2.0 V to 3.5 V
- Integrated reference buffer generates virtual ground
- Rail-to-rail output
- Internal RFI filter
- 8 kV HBM ESD rating
- Shutdown pin
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Fitness and activity heart rate monitors
- Portable ECG
- Remote health monitors
- Gaming peripherals
- Biopotential signal acquisition

FUNCTIONAL BLOCK DIAGRAM

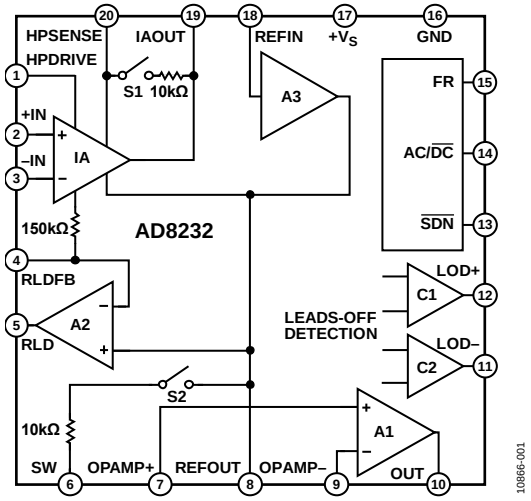


Figure 1.

GENERAL DESCRIPTION

The AD8232 is an integrated signal conditioning block for ECG and other biopotential measurement applications. It is designed to extract, amplify, and filter small biopotential signals in the presence of noisy conditions, such as those created by motion or remote electrode placement. This design allows for an ultralow power analog-to-digital converter (ADC) or an embedded microcontroller to acquire the output signal easily.

The AD8232 can implement a two-pole high-pass filter for eliminating motion artifacts and the electrode half-cell potential. This filter is tightly coupled with the instrumentation architecture of the amplifier to allow both large gain and high-pass filtering in a single stage, thereby saving space and cost.

An uncommitted operational amplifier enables the AD8232 to create a three-pole low-pass filter to remove additional noise. The user can select the frequency cutoff of all filters to suit different types of applications.

To improve common-mode rejection of the line frequencies in the system and other undesired interferences, the AD8232 includes an amplifier for driven lead applications, such as right leg drive (RLD).

The AD8232 includes a fast restore function that reduces the duration of otherwise long settling tails of the high-pass filters. After an abrupt signal change that rails the amplifier (such as a leads off condition), the AD8232 automatically adjusts to a higher filter cutoff. This feature allows the AD8232 to recover quickly, and therefore, to take valid measurements soon after connecting the electrodes to the subject.

The AD8232 is available in a 4 mm × 4 mm, 20-lead LFCSP package. Performance is specified from 0°C to 70°C and is operational from −40°C to +85°C.

Rev. B
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD8232* PRODUCT PAGE QUICK LINKS

Last Content Update: 06/02/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD8232 Evaluation Board

DOCUMENTATION

Data Sheet

- AD8232: Single-Lead, Heart Rate Monitor Front End Data Sheet

Technical Books

- A Designer's Guide to Instrumentation Amplifiers, 3rd Edition, 2006

User Guides

- UG-514: Evaluating the AD8232 Single-Lead Heart Rate Monitor Front End

TOOLS AND SIMULATIONS

- AD8232/AD8233 Filter Design Tool
- AD8232 SPICE Macro Model

REFERENCE MATERIALS

Press

- Analog Devices Introduces Industry's Lowest Power, Smallest, Single-Lead Heart-Rate Monitor Analog Front End

Technical Articles

- Home is Where the Heart Is
- MS-2385: Predicting and Finding Your Limits!

DESIGN RESOURCES

- AD8232 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8232 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

3/2017—Rev. A to Rev. B

Updated Outline Dimensions ... 27
Changes to Ordering Guide ... 27

2/2013—Rev. 0 to Rev. A

Changes to Table 1 ... 4
Changes to Table 2 ... 6
Change to Figure 17 ... 9
Changes to Figure 22 and Figure 25 ... 11
Changes to Figure 34 and Figure 36 ... 14
Changes to Figure 45, Architecture Overview Section, and Instrumentation Amplifier Section ... 17
Changes to Right Leg Drive Amplifier Section, Reference Buffer Section, Fast Restore Circuit Section, and Figure 48; Added Figure 46, Renumbered Sequentially ... 18
Changes to Figure 49 ... 19
Changes to AC Leads Off Detection Section and Standby Operation Section ... 20
Changes to Input Referred Offsets Section ... 21
Changes to Figure 53 and High-Pass Filtering Section ... 22
Changes to Additional High-Pass Filtering Options Section; Added Table 4 ... 23
Changes to Low-Pass Filtering and Gain Section; Added Driving Analog-to-Digital Converters Section and Figure 61 ... 24
Changes to Figure 62, Figure 64, and Heart Rate Measurement Next to the Heart Section ... 25
Changes to Exercise Application: Heart Rate Measured at the Hands and Figure 66 ... 26
Changes to Figure 68 ... 27

8/2012—Revision 0: Initial Version

SPECIFICATIONS

V_S = 3 V, V_{REF} = 1.5 V, V_{CM} = 1.5 V, T_A = 25°C, FR=low, SDN=high, AC/$\overline{DC}$ = low, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER						
Common-Mode Rejection Ratio, DC to 60 Hz	CMRR	V_{CM} = 0.35 V to 2.85 V, V_{DIFF} = 0 V	80	86		dB
		V_{CM} = 0.35 V to 2.85 V, V_{DIFF} = ±0.3 V		80		dB
Power Supply Rejection Ratio	PSRR	V_S = 2.0 V to 3.5 V	76	90		dB
Offset Voltage (RTI)	V_{OS}					
Instrumentation Amplifier Inputs				3	8	mV
DC Blocking Input[1]				5	50	µV
Average Offset Drift						
Instrumentation Amplifier Inputs				10		µV/°C
DC Blocking Input[1]				0.05		µV/°C
Input Bias Current	I_B			50	200	pA
		T_A = 0°C to 70°C		1		nA
Input Offset Current	I_{OS}			25	100	pA
		T_A = 0°C to 70°C		1		nA
Input Impedance						
Differential				10||7.5		GΩ||pF
Common Mode				5||15		GΩ||pF
Input Voltage Noise (RTI)						
Spectral Noise Density		f = 1 kHz		100		nV/√Hz
Peak-to-Peak Voltage Noise		f = 0.1 Hz to 10 Hz		12		µV p-p
		f = 0.5 Hz to 40 Hz		14		µV p-p
Input Voltage Range		T_A = 0°C to 70°C	0.2		$+V_S$	V
DC Differential Input Range	V_{DIFF}		−300		+300	mV
Output						
Output Swing		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current	I_{OUT}			6.3		mA
Gain	A_V			100		V/V
Gain Error		V_{DIFF} = 0 V		0.4		%
		V_{DIFF} = −300 mV to +300 mV		1	3.5	%
Average Gain Drift		T_A = 0°C to 70°C		12		ppm/°C
Bandwidth	BW			2		kHz
RFI Filter Cutoff (Each Input)				1		MHz
OPERATIONAL AMPLIFIER (A1)						
Offset Voltage	V_{OS}			1	5	mV
Average TC		T_A = 0°C to 70°C		5		µV/°C
Input Bias Current	I_B			100		pA
		T_A = 0°C to 70°C		1		nA
Input Offset Current	I_{OS}			100		pA
		T_A = 0°C to 70°C		1		nA
Input Voltage Range			0.1		$+V_S$ − 0.1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.5 V to 2.5 V		100		dB
Power Supply Rejection Ratio	PSRR			100		dB
Large Signal Voltage Gain	A_{VO}			110		dB
Output Voltage Range		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current Limit	I_{OUT}			12		mA
Gain Bandwidth Product	GBP			100		kHz
Slew Rate	SR			0.02		V/µs
Voltage Noise Density (RTI)	e_n	f = 1 kHz		60		nV/√Hz
Peak-to-Peak Voltage Noise (RTI)	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		6		µV p-p
		f = 0.5 Hz to 40 Hz		8		µV p-p

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RIGHT LEG DRIVE AMPLIFIER (A2)						
Output Swing		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current	I_{OUT}			11		mA
Integrator Input Resistor			120	150	180	kΩ
Gain Bandwidth Product	GDP			100		kHz
REFERENCE BUFFER (A3)						
Offset Error	V_{OS}	R_L > 50 kΩ		1		mV
Input Bias Current	I_B			100		pA
Short-Circuit Current Limit	I_{OUT}			12		mA
Voltage Range		R_L = 50 kΩ	0.1		$+V_S$ − 0.7	V
DC LEADS OFF COMPARATORS						
Threshold Voltage				$+V_S$ − 0.5		V
Hysteresis				60		mV
Propagation Delay				0.5		µs
AC LEADS OFF DETECTOR						
Square Wave Frequency	F_{AC}		50	100	175	kHz
Square Wave Amplitude	I_{AC}			200		nA p-p
Impedance Threshold		Between +IN and −IN	10	20		MΩ
Detection Delay				110		µs
FAST RESTORE CIRCUIT						
Switches		S1 and S2				
On Resistance	R_{ON}		8	10	12	kΩ
Off Leakage				100		pA
Window Comparator						
Threshold Voltage		From either rail		50		mV
Propagation Delay				2		µs
Switch Timing Characteristics						
Feedback Recovery Switch On Time	t_{SW1}			110		ms
Filter Recovery Switch On Time	t_{SW2}			55		ms
Fast Restore Reset	t_{RST}			2		µs
LOGIC INTERFACE						
Input Characteristics						
Input Voltage (AC/$\overline{DC}$ and FR)						
Low	V_{IL}			1.24		V
High	V_{IH}			1.35		V
Input Voltage ($\overline{SDN}$)						
Low	V_{IL}			2.1		V
High	V_{IH}			0.5		V
Output Characteristics		LOD+ and LOD− terminals				
Output Voltage						
Low	V_{OL}			0.05		V
High	V_{OH}			2.95		V
SYSTEM SPECIFICATIONS						
Quiescent Supply Current				170	230	µA
		T_A = 0°C to 70°C		210		µA
Shutdown Current				40	500	nA
		T_A = 0°C to 70°C		100		nA
Supply Range			2.0		3.5	V
Specified Temperature Range			0		70	°C
Operational Temperature Range			−40		+85	°C

[1] Offset referred to the input of the instrumentation amplifier inputs. See the Input Referred Offsets section for additional information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	3.6 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage, Any Terminal[1]	$+V_S$ + 0.3 V
Minimum Voltage, Any Terminal[1]	−0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	140°C
θ_{JA} Thermal Impedance[2]	48°C/W
θ_{JC} Thermal Impedance	4.4°C/W
ESD Rating	
Human Body Model (HBM)	8 kV
Charged Device Model (FICDM)	1.25 kV
Machine Model (MM)	200 V

[1] This level or the maximum specified supply voltage, whichever is the lesser, indicates the superior voltage limit for any terminal. If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to less than 5 mA.
[2] θ_{JA} is specified for a device in free air on a 4-layer JEDEC board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

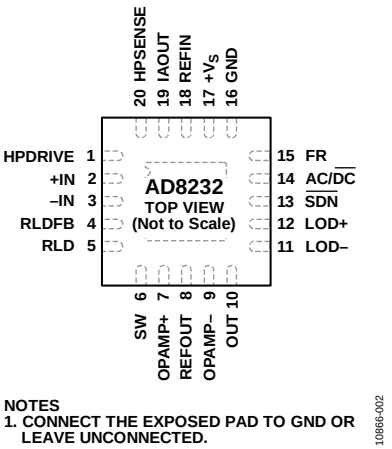


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	HPDRIVE	High-Pass Driver Output. Connect HPDRIVE to the capacitor in the first high-pass filter. The AD8232 drives this pin to keep HPSENSE at the same level as the reference voltage.
2	+IN	Instrumentation Amplifier Positive Input. +IN is typically connected to the left arm (LA) electrode.
3	−IN	Instrumentation Amplifier Negative Input. −IN is typically connected to the right arm (RA) electrode.
4	RLDFB	Right Leg Drive Feedback Input. RLDFB is the feedback terminal for the right leg drive circuit.
5	RLD	Right Leg Drive Output. Connect the driven electrode (typically, right leg) to the RLD pin.
6	SW	Fast Restore Switch Terminal. Connect this terminal to the output of the second high-pass filter.
7	OPAMP+	Operational Amplifier Noninverting Input.
8	REFOUT	Reference Buffer Output. The instrumentation amplifier output is referenced to this potential. Use REFOUT as a virtual ground for any point in the circuit that needs a signal reference.
9	OPAMP−	Operational Amplifier Inverting Input.
10	OUT	Operational Amplifier Output. The fully conditioned heart rate signal is present at this output. OUT can be connected to the input of an ADC.
11	LOD−	Leads Off Comparator Output. In dc leads off detection mode, LOD− is high when the electrode to −IN is disconnected, and it is low when connected. In ac leads off detection mode, LOD− is always low.
12	LOD+	Leads Off Comparator Output. In dc leads off detection mode, LOD+ is high when the +IN electrode is disconnected, and it is low when connected. In ac leads off detection mode, LOD+ is high when either the −IN or +IN electrode is disconnected, and it is low when both electrodes are connected.
13	$\overline{\text{SDN}}$	Shutdown Control Input. Drive $\overline{\text{SDN}}$ low to enter the low power shutdown mode.
14	AC/$\overline{\text{DC}}$	Leads Off Mode Control Input. Drive the AC/$\overline{\text{DC}}$ pin low for dc leads off mode. Drive the AC/$\overline{\text{DC}}$ pin high for ac leads off mode.
15	FR	Fast Restore Control Input. Drive FR high to enable fast recovery mode; otherwise, drive it low.
16	GND	Power Supply Ground.
17	$+V_S$	Power Supply Terminal.
18	REFIN	Reference Buffer Input. Use REFIN, a high impedance input terminal, to set the level of the reference buffer.
19	IAOUT	Instrumentation Amplifier Output Terminal.
20	HPSENSE	High-Pass Sense Input for Instrumentation Amplifier. Connect HPSENSE to the junction of R and C that sets the corner frequency of the dc blocking circuit.
	EP	Exposed Pad. Connect the exposed pad to GND or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3 V, V_{REF} = 1.5 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

INSTRUMENTATION AMPLIFIER PERFORMANCE CURVES

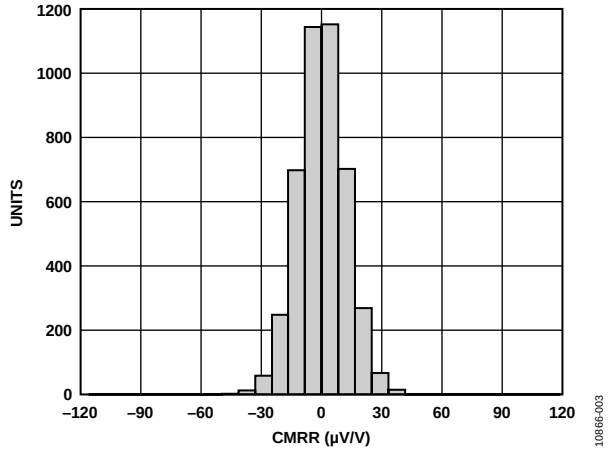


Figure 3. Instrumentation Amplifier CMRR Distribution

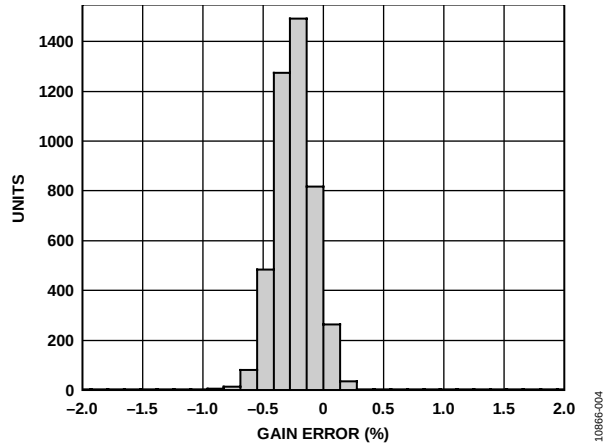


Figure 4. Instrumentation Amplifier Gain Error Distribution

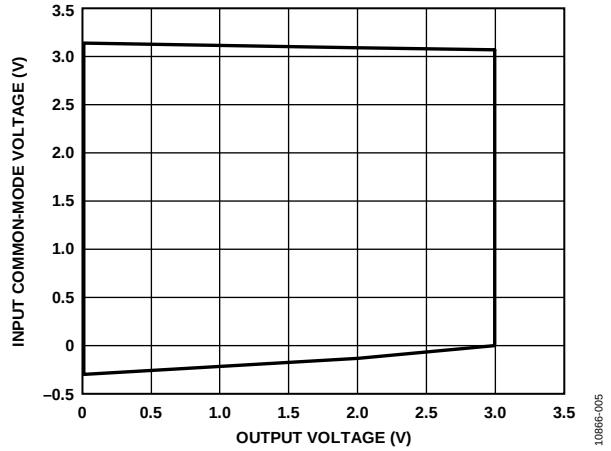


Figure 5. Instrumentation Amplifier
Input Common-Mode Range vs. Output Voltage

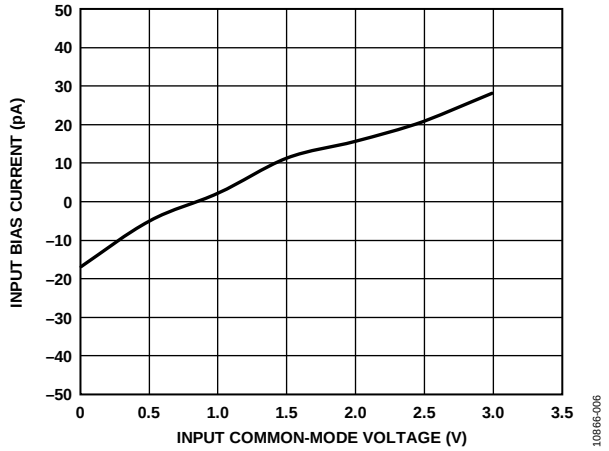


Figure 6. Instrumentation Amplifier Input Bias Current vs. CMV

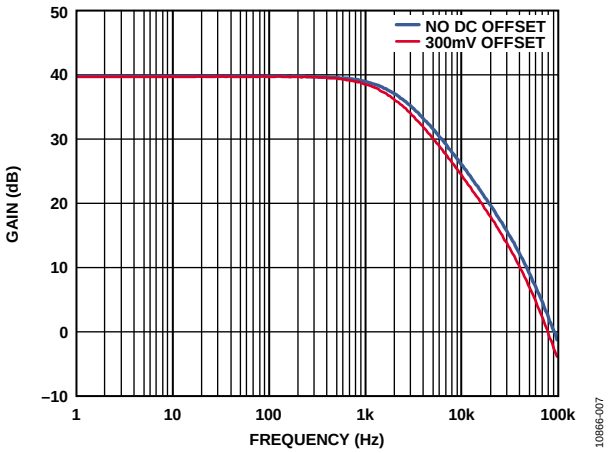


Figure 7. Instrumentation Amplifier Gain vs. Frequency

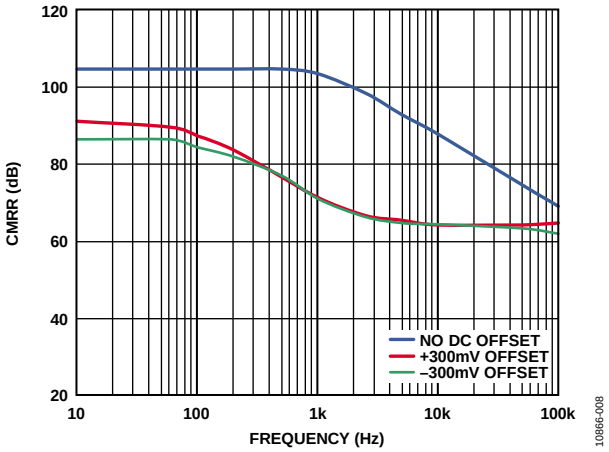


Figure 8. Instrumentation Amplifier CMRR vs. Frequency, RTI

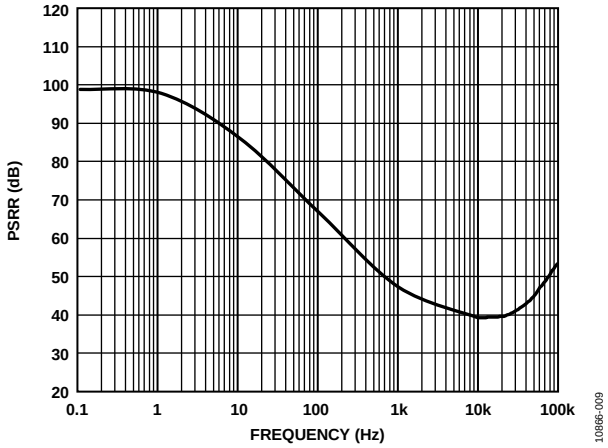


Figure 9. Instrumentation Amplifier PSRR vs. Frequency

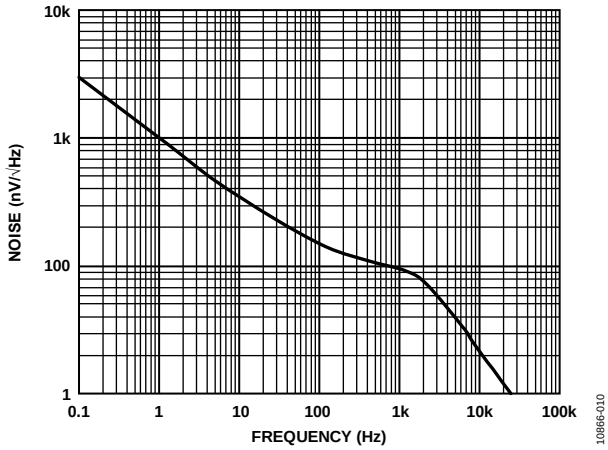


Figure 10. Instrumentation Amplifier Voltage Noise Spectral Density (RTI)

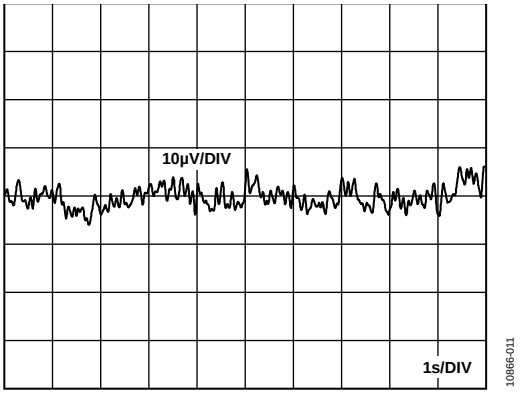


Figure 11. Instrumentation Amplifier 0.1 Hz to 10 Hz Noise

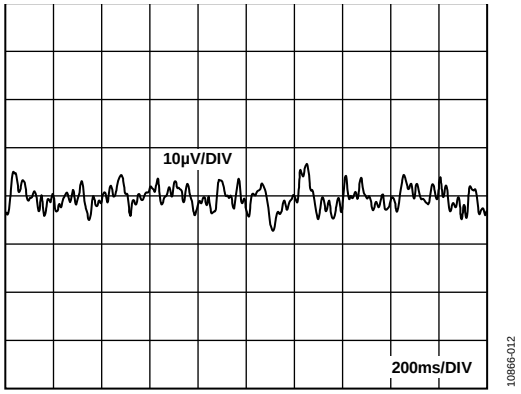


Figure 12. Instrumentation Amplifier 0.5 Hz to 40 Hz Noise

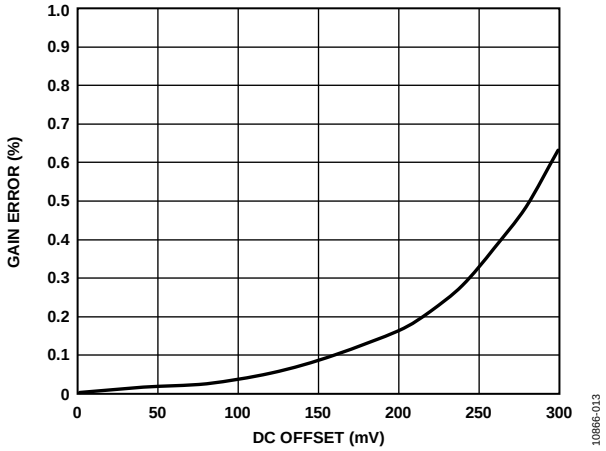


Figure 13. Instrumentation Amplifier Gain Error vs. DC Offset

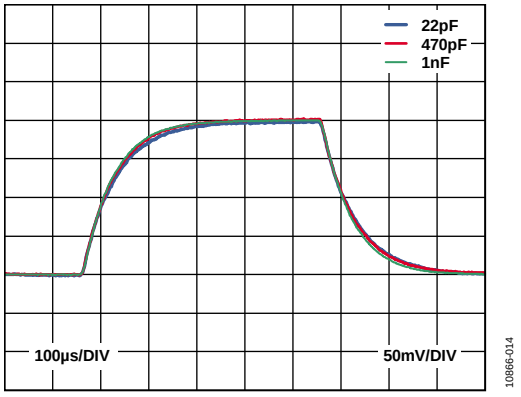


Figure 14. Instrumentation Amplifier Small Signal Pulse Response

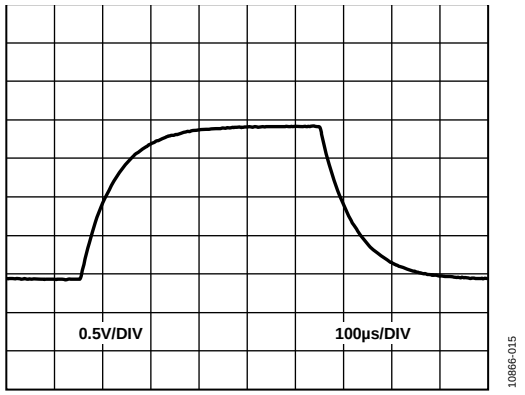


Figure 15. Instrumentation Amplifier Large Signal Pulse Response

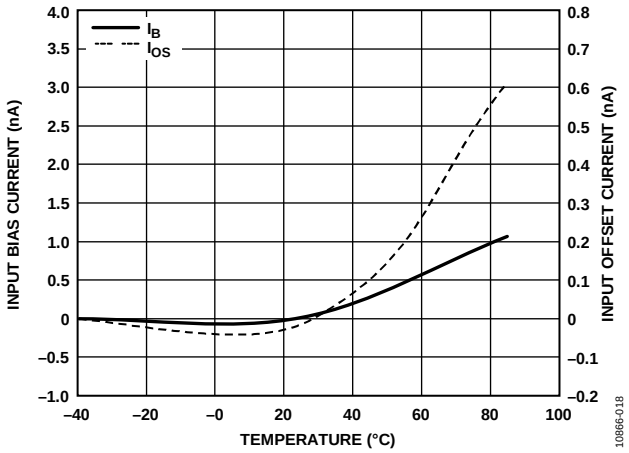


Figure 18. Instrumentation Amplifier
Input Bias Current and Input Offset Current vs. Temperature

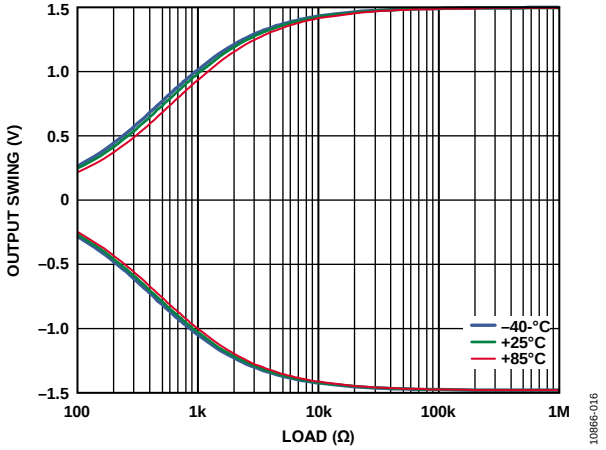


Figure 16. Instrumentation Amplifier Output Swing vs. Load

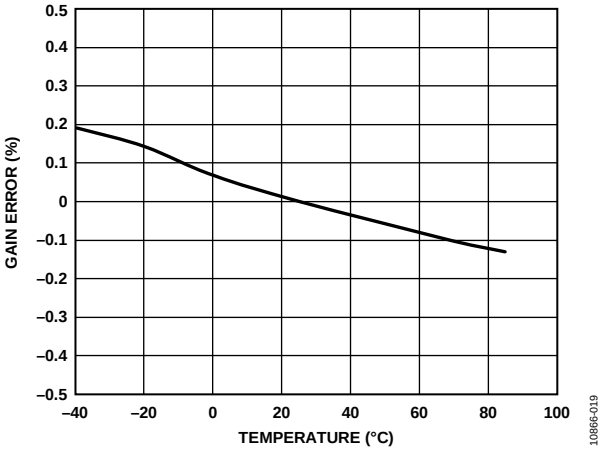


Figure 19. Instrumentation Amplifier Gain Error vs. Temperature

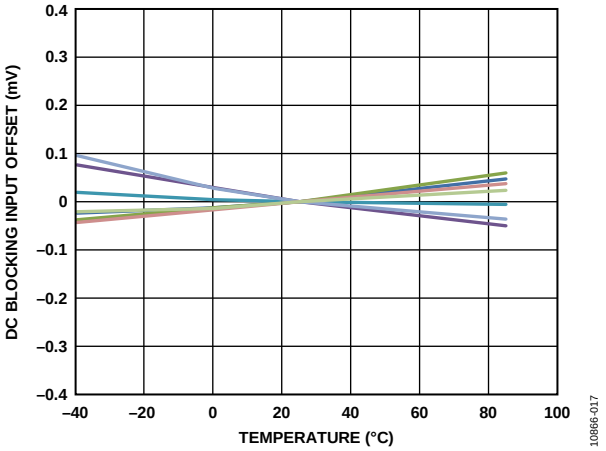


Figure 17. Instrumentation Amplifier DC Blocking Input Offset Drift

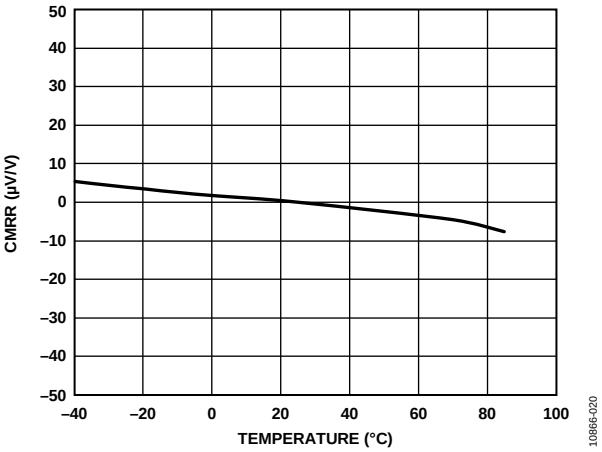


Figure 20. Instrumentation Amplifier CMRR vs. Temperature

OPERATIONAL AMPLIFIER PERFORMANCE CURVES

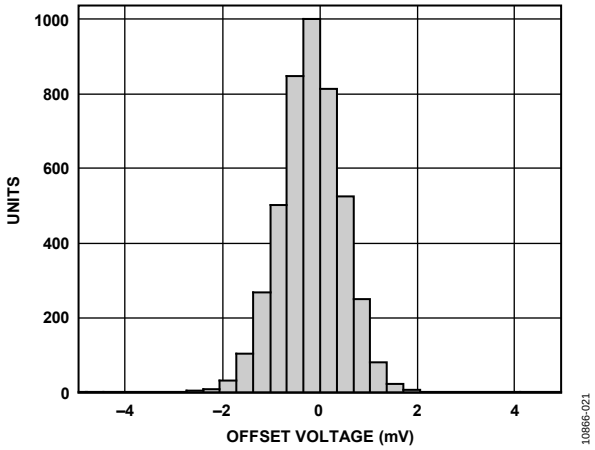


Figure 21. Operational Amplifier Offset Distribution

Figure 24. Operational Amplifier Large Signal Transient Response

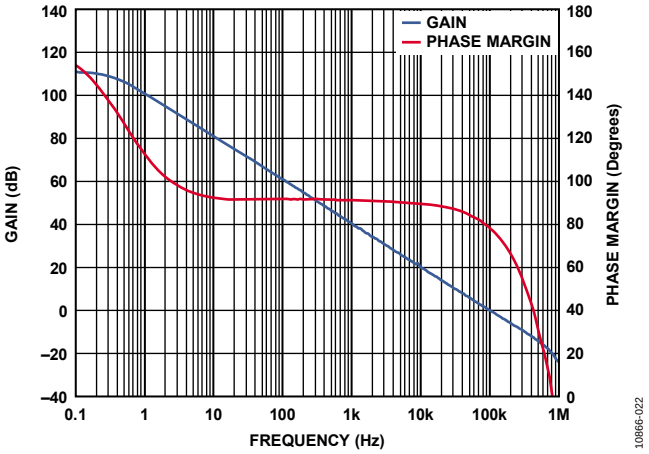


Figure 22. Operational Amplifier Open-Loop Gain and Phase vs. Frequency

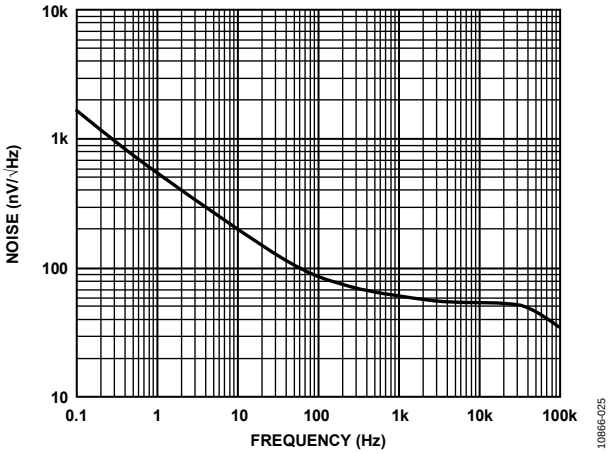


Figure 25. Operational Amplifier Voltage Spectral Noise Density vs. Frequency

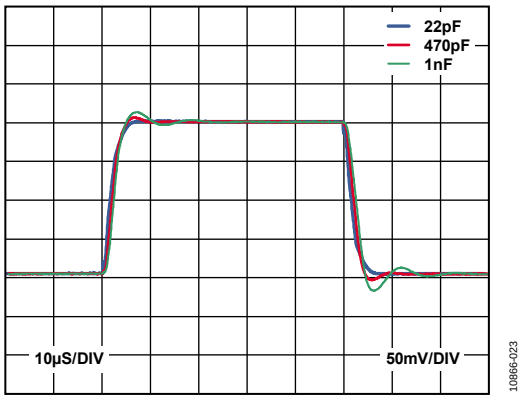


Figure 23. Operational Amplifier Small Signal Response for Various Capacitive Loads

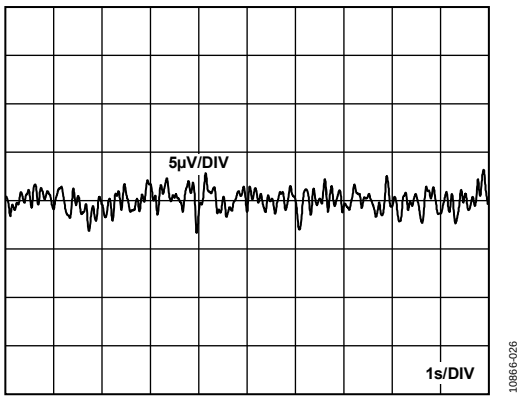


Figure 26. Operational Amplifier 0.1 Hz to 10 Hz Noise

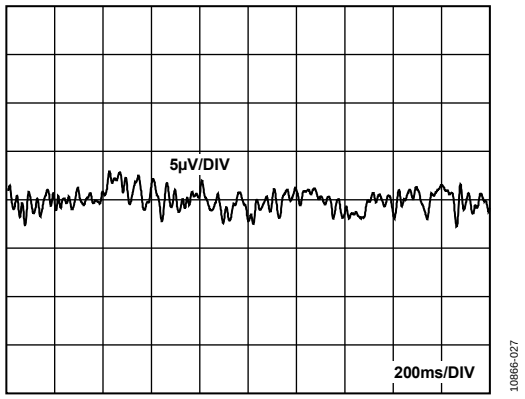


Figure 27. Operational Amplifier 0.5 Hz to 40 Hz Noise

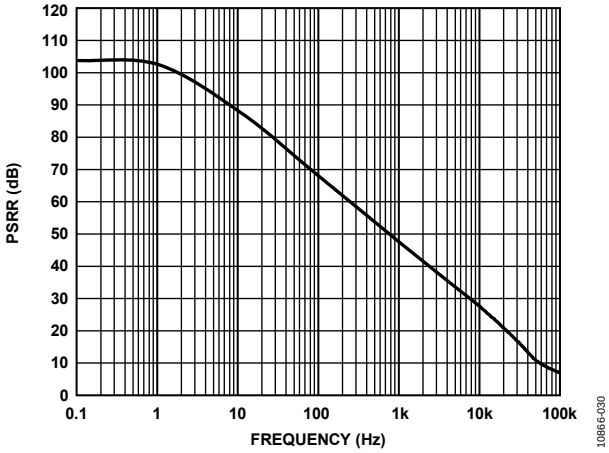


Figure 30. Operational Amplifier Power Supply Rejection Ratio

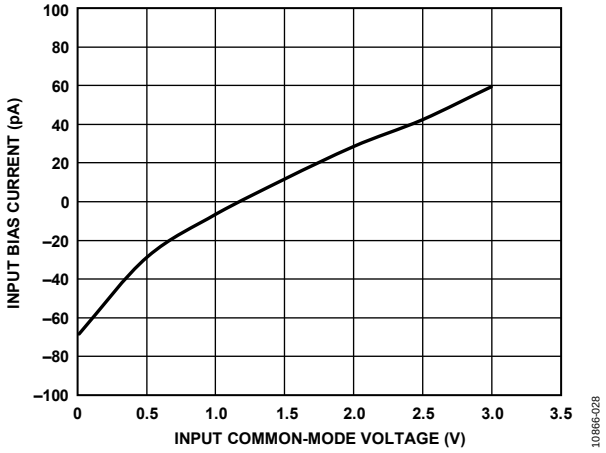


Figure 28. Operational Amplifier Bias Current vs. Input Common-Mode Voltage

Figure 31. Operational Amplifier Load Transient Response (100 µA Load Change)

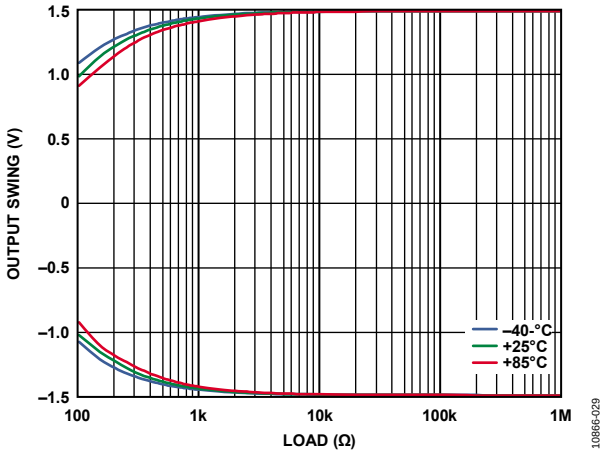


Figure 29. Operational Amplifier Output Voltage Swing vs. Output Current

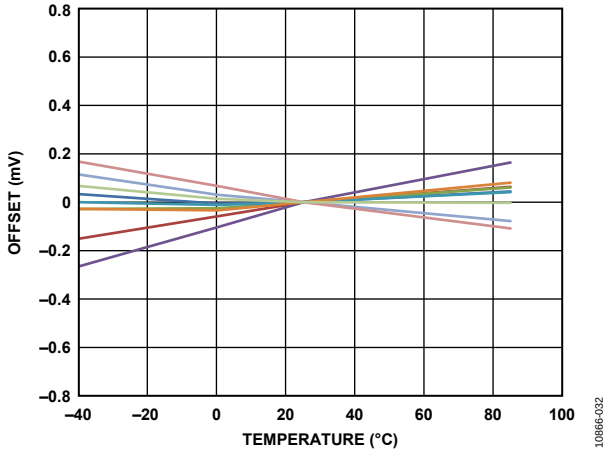


Figure 32. Operational Amplifier Offset vs. Temperature

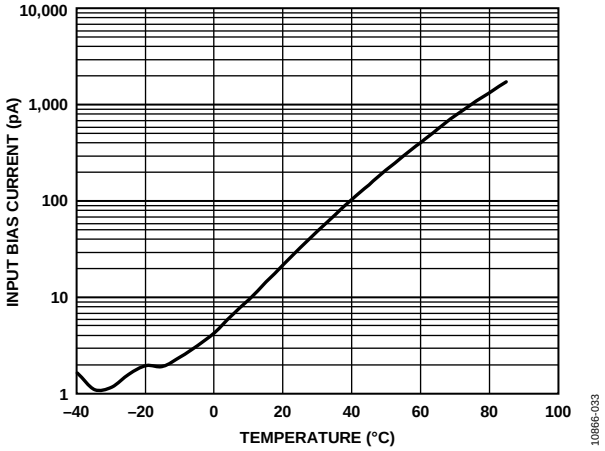


Figure 33. Operational Amplifier Bias Current vs. Temperature

RIGHT LEG DRIVE (RLD) AMPLIFIER PERFORMANCE CURVES

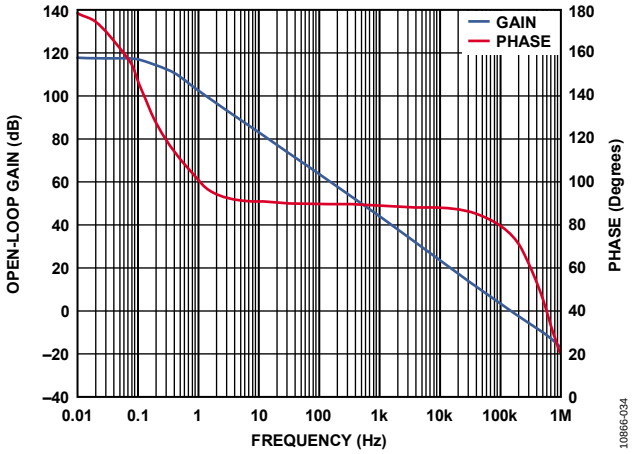


Figure 34. RLD Amplifier Open-Loop Gain and Phase vs. Frequency

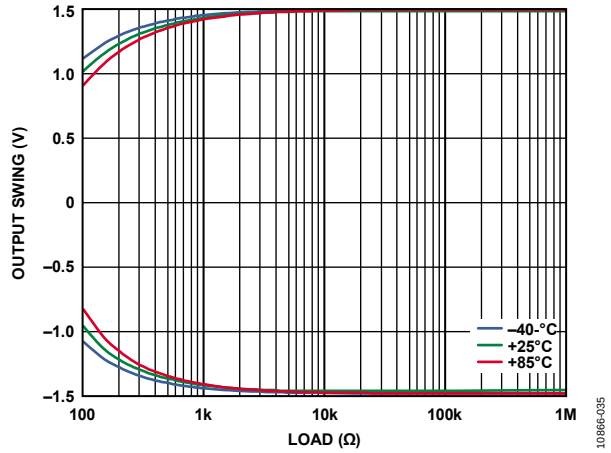


Figure 35. RLD Amplifier Output Voltage Swing vs. Output Current

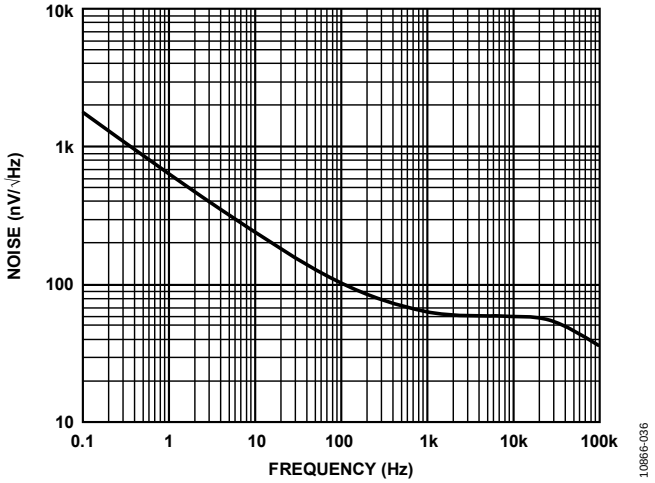


Figure 36. RLD Amplifier Voltage Spectral Noise Density vs. Frequency

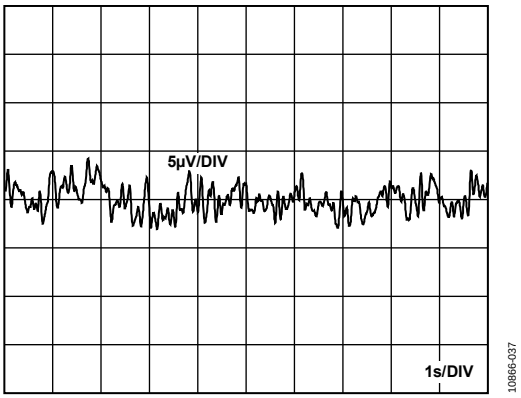


Figure 37. RLD Amplifier 0.1 Hz to 10 Hz Noise

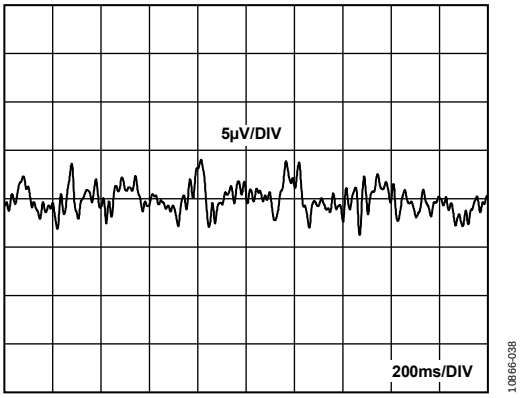


Figure 38. RLD Amplifier 0.5 Hz to 40 Hz Noise

REFERENCE BUFFER PERFORMANCE CURVES

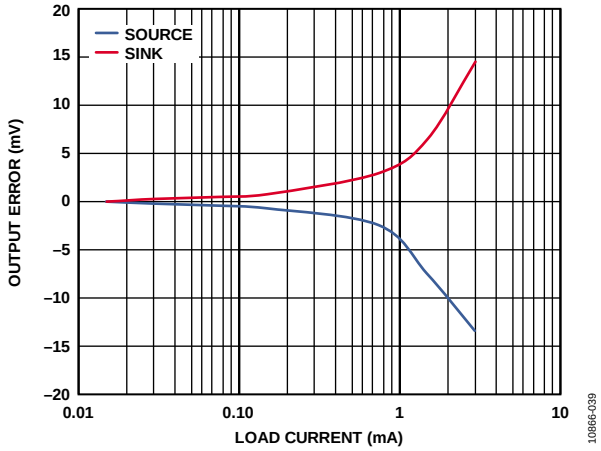


Figure 39. Reference Buffer Load Regulation

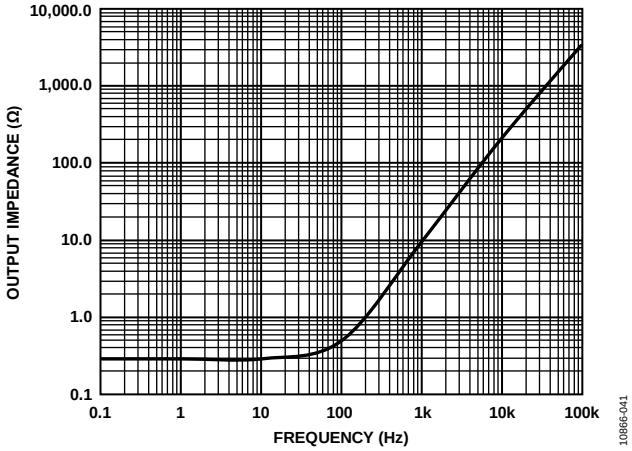


Figure 41. Reference Buffer Output Impedance vs. Frequency

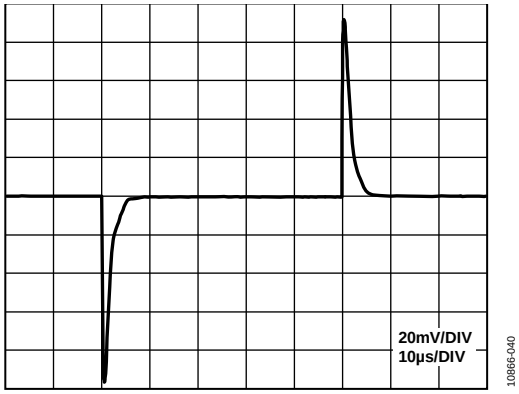


Figure 40. Reference Buffer Load Transient Response (100 µA Load Change)

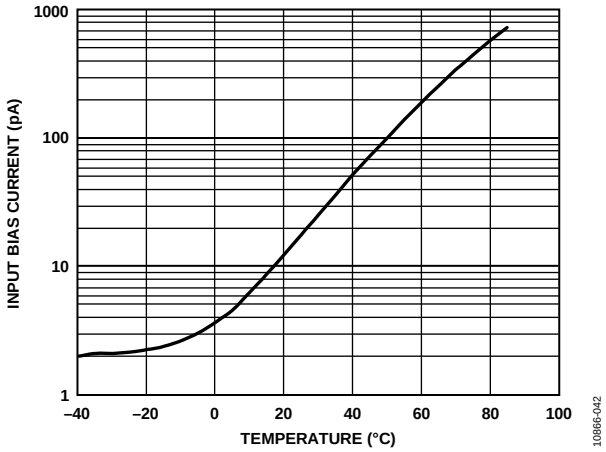


Figure 42. Reference Buffer Bias Current vs. Temperature

SYSTEM PERFORMANCE CURVES

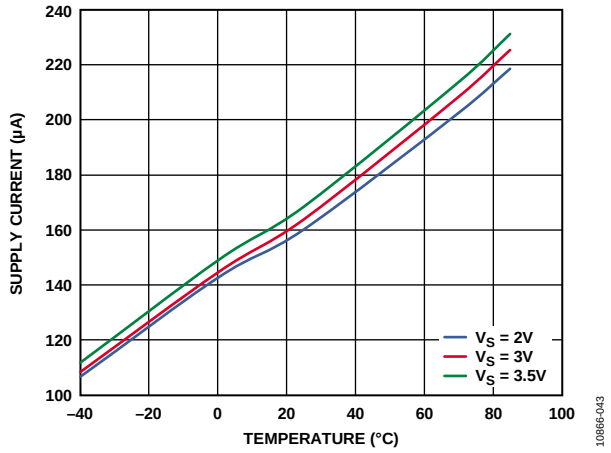


Figure 43. Supply Current vs. Temperature

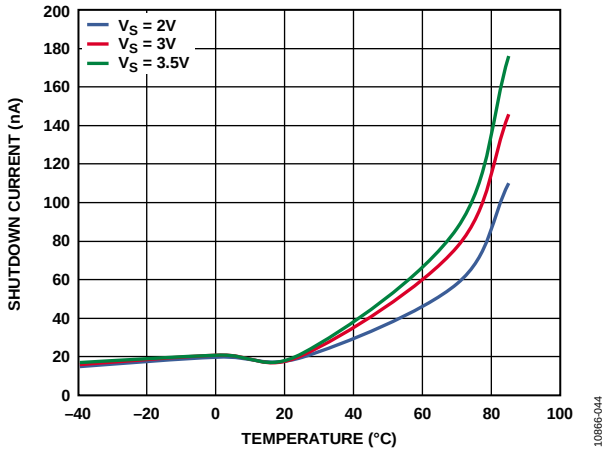


Figure 44. Shutdown Current vs. Temperature

THEORY OF OPERATION

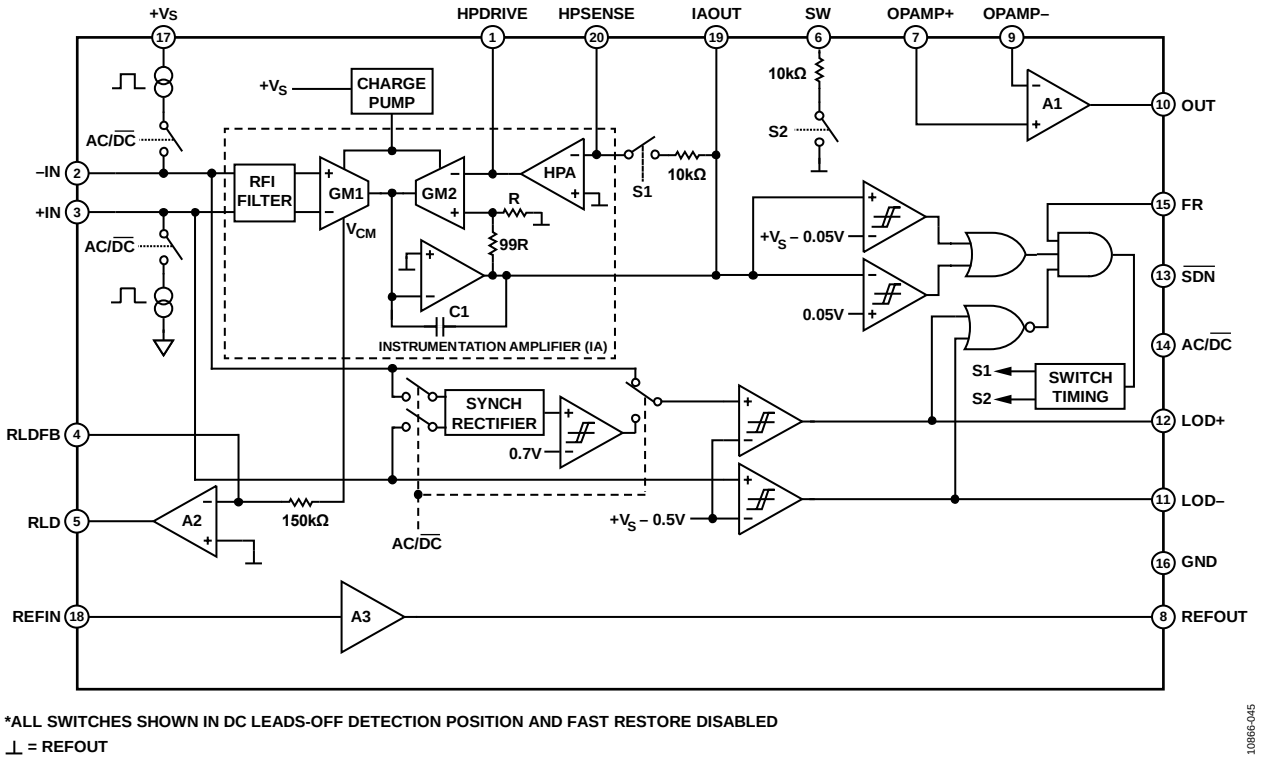


Figure 45. Simplified Schematic Diagram

ARCHITECTURE OVERVIEW

The AD8232 is an integrated front end for signal conditioning of cardiac biopotentials for heart rate monitoring. It consists of a specialized instrumentation amplifier (IA), an operational amplifier (A1), a right leg drive amplifier (A2), and a midsupply reference buffer (A3). In addition, the AD8232 includes leads off detection circuitry and an automatic fast restore circuit that brings back the signal shortly after leads are reconnected.

The AD8232 contains a specialized instrumentation amplifier that amplifies the ECG signal while rejecting the electrode half-cell potential on the same stage. This is possible with an indirect current feedback architecture, which reduces size and power compared with traditional implementations

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is shown in Figure 45 as comprised by two well-matched transconductance amplifiers (GM1 and GM2), the dc blocking amplifier (HPA), and an integrator formed by C1 and an op amp. The transconductance amplifier, GM1, generates a current that is proportional to the voltage present at its inputs. When the feedback is satisfied, an equal voltage appears across the inputs of the transconductance amplifier, GM2, thereby matching the current generated by GM1. The difference generates an error current that is integrated across Capacitor C1. The resulting voltage appears at the output of the instrumentation amplifier.

The feedback of the amplifier is applied via GM2 through two separate paths: the two resistors divide the output signal to set an overall gain of 100, whereas the dc blocking amplifier integrates any deviation from the reference level. Consequently, dc offsets as large as ±300 mV across the GM1 inputs appear inverted and with the same magnitude across the inputs of GM2, all without saturating the signal of interest.

To increase the common-mode voltage range of the instrumentation amplifier, a charge pump boosts the supply voltage for the two transconductance amplifiers. This further prevents saturation of the amplifier in the presence of large common-mode signals, such as line interference. The charge pump runs from an internal oscillator, the frequency of which is set around 500 kHz.

OPERATIONAL AMPLIFIER

This general-purpose operational amplifier (A1) is a rail-to-rail device that can be used for low-pass filtering and to add additional gain. The following sections provide details and example circuits that use this amplifier.

RIGHT LEG DRIVE AMPLIFIER

The right leg drive (RLD) amplifier inverts the common-mode signal that is present at the instrumentation amplifier inputs. When the right leg drive output current is injected into the subject, it counteracts common-mode voltage variations, thus improving the common-mode rejection of the system.

The common-mode signal that is present across the inputs of the instrumentation amplifier is derived from the transconductance amplifier, GM1. It is then connected to the inverting input of A2 through a 150 kΩ resistor.

An integrator can be built by connecting a capacitor between the RLD FB and RLD terminals. A good starting point is a 1 nF capacitor, which places the crossover frequency at about 1 kHz (the frequency at which the amplifier has an inverting unity gain). This configuration results in about 26 dB of loop gain available at a frequency range from 50 Hz to 60 Hz for common-mode line rejection. Higher capacitor values reduce the crossover frequency, thereby reducing the gain that is available for rejection and, consequently, increasing the line noise. Lower capacitor values move the crossover frequency to higher frequencies, allowing increased gain. The tradeoff is that with higher gain, the system can become unstable and saturate the output of the right leg amplifier.

Note that when using this amplifier to drive an electrode, there should be a resistor in series with the output to limit the current to be always less than 10uA even in fault conditions. For example, if the supply used is 3.0V, this resistor should be greater than 330kΩ to account for component and supply variations.

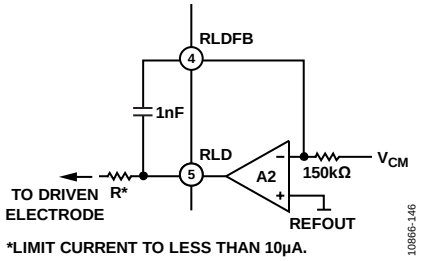


Figure 46. Typical Configuration of Right-Leg Drive Circuit

In two-electrode configurations, RLD can be used to bias the inputs through 10MΩ resistors as described in the Leads Off Detection section. If left unused, it is recommended to configure A2 as a follower by connecting RLDFB directly to RLD.

REFERENCE BUFFER

The AD8232 operates from a single supply. To simplify the design of single-supply applications, the AD8232 includes a reference buffer to create a virtual ground between the supply voltage and the system ground. The signals present at the output of the instrumentation amplifier are referenced around this voltage. For example, if there is zero differential input voltage, the voltage at the output of the instrumentation amplifier is this reference voltage.

The reference voltage level is set at the REFIN pin. It can be set with a voltage divider or by driving the REFIN pin from some other point in the circuit (for example, from the ADC reference). The voltage is available at the REFOUT pin for the filtering circuits or for an ADC input.

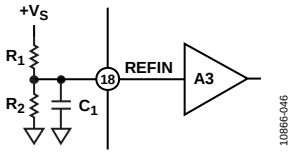


Figure 47. Setting the Internal Reference

To limit the power consumption of the voltage divider, the use of large resistors is recommended, such as 10 MΩ. The designer must keep in mind that high resistor values make it easier for interfering signals to appear at the input of the reference buffer. To minimize noise pickup, it is recommended to place the resistors close to each other and as near as possible to the REFIN terminal. Furthermore, use a capacitor in parallel with the lower resistor on the divider for additional filtering, as shown in Figure 47. Keep in mind that a large capacitor results in better noise filtering but it takes longer to settle the reference after power-up. The total time it takes the reference to settle within 1% can be estimated with the formula

$$t_{SETTLE\_REFERENCE} = 5 \times \frac{R1R2C1}{R1 + R2}$$

Note that disabling the AD8232 with the shutdown terminal does not discharge this capacitor.

FAST RESTORE CIRCUIT

Because of the low cutoff frequency used in high-pass filters in ECG applications, signals may require several seconds to settle. This settling time can result in a frustrating delay for the user after a step response: for example, when the electrodes are first connected.

This fast restore function is implemented internally, as shown in Figure 48. The output of the instrumentation amplifier is connected to a window comparator. The window comparator detects a saturation condition at the output of the instrumentation amplifier when its voltage approaches 50 mV from either supply rail.

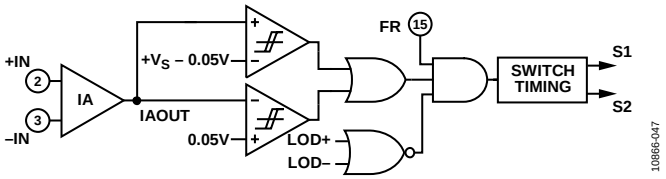


Figure 48. Fast Restore Circuit

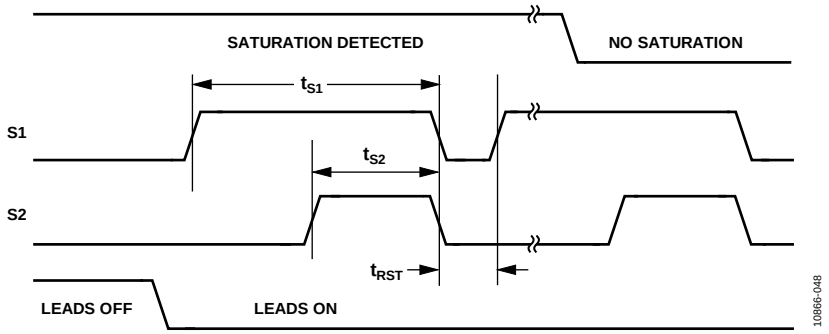


Figure 49. Timing Diagram for Fast Restore Switches (Time Base Not to Scale)

If this saturation condition is present when both input electrodes are attached to the subject, the comparator triggers a timing circuit that automatically closes Switch S1 and Switch S2 (see Figure 49 for a timing diagram).

These two switches (S1 and S2) enable two different 10 kΩ resistor paths: one between HPSENSE and IAOUT and another between SW and REFOUT. During the time Switch S1 and Switch S2 are enabled, these internal resistors appear in parallel with their corresponding external resistors forming high-pass filters. The result is that the equivalent lower resistance shifts the pole to a higher frequency, delivering a quicker settling time. Note that the fast restore settling time depends on how quickly the internal 10 kΩ resistors of the AD8232 can drain the capacitors in the high-pass circuit. Smaller capacitor values result in a shorter settling time.

If, by the end of the timing, the saturation condition persists, the cycle repeats. Otherwise, the AD8232 returns to its normal operation. If either of the leads off comparator outputs is indicating that an electrode has been disconnected, the timing circuit is prevented from triggering because it is assumed that no valid signal is present. To disable fast restore, drive the FR pin low or tie it permanently to GND.

LEADS OFF DETECTION

The AD8232 includes leads off detection. It features ac and dc detection modes optimized for either two- or three-electrode configurations, respectively.

DC Leads Off Detection

The dc leads off detection mode is used in three-electrode configurations only. It works by sensing when either instrumentation amplifier input voltage is within 0.5 V from the positive rail. In this case, each input must have a pull-up resistor connected to the positive supply. During normal operation, the subject's potential must be inside the common-mode range of the instrumentation amplifier, which is only possible if a third electrode is connected to the output of the right leg drive amplifier.

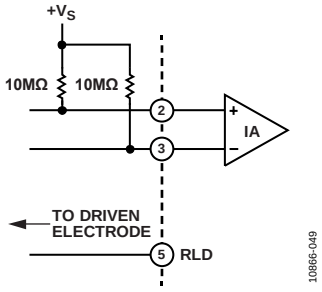


Figure 50. Circuit Configuration for DC Leads Off Detection

Because in dc leads off mode the AD8232 checks each input individually, it is possible to indicate which electrode is disconnected. The AD8232 indicates which electrode is disconnected by setting the corresponding LOD− or LOD+ pin high. To use this mode, connect the AC/$\overline{DC}$ pin to ground.

AC Leads Off Detection

The ac leads off detection mode is useful when using two electrodes only (it does not require the use of a driven electrode). In this case, a conduction path must exist between the two electrodes, which is usually formed by two resistors, as shown in Figure 51.

These resistors also provide a path for bias return on each input. Connect each resistor to REFOUT or RLD to maintain the inputs within the common-mode range of the instrumentation amplifier.

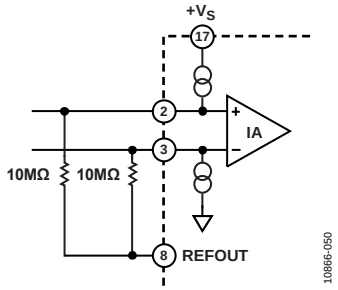


Figure 51. Circuit Configuration for AC Leads Off Detection

The AD8232 detects when an electrode is disconnected by forcing a small 100 kHz current into the input terminals. This current flows through the external resistors from IN+ to IN− and develops a differential voltage across the inputs, which is then synchronously detected and compared to an internal threshold. The recommended value for these external resistors is 10 MΩ. Low resistance values make the differential drop too low to be detected and lower the input impedance of the amplifier. When the electrodes are attached to the subject, the impedance of this path should be less than 3 MΩ to maintain the drop below the comparator's threshold.

As opposed to the dc leads off detection mode, the AD8232 is able to determine only that an electrode has lost its connection, not which one. During such an event, the LOD+ pin goes high. In this mode, the LOD− pin is not used and remains in a logic low state. To use the ac leads off mode, tie the AC/$\overline{DC}$ pin to the positive supply rail.

Note that while REFOUT is at a constant voltage value, using the RLD output as the input bias may be more effective in rejecting common-mode interference.

STANDBY OPERATION

The AD8232 includes a shutdown pin ($\overline{SDN}$) that further enhances the flexibility and ease of use in portable applications where power consumption is critical. A logic level signal can be applied to this pin to switch to shutdown mode, even when the supply is still on.

Driving the $\overline{SDN}$ pin low places the AD8232 in shutdown mode and draws less than 200 nA of supply current, offering considerable power savings. To enter normal operation, drive $\overline{SDN}$ high; when not using this feature, permanently tie $\overline{SDN}$ to $+V_S$.

During shutdown operation, the AD8232 is not able to maintain the REFOUT voltage, but it does not drain the REFIN voltage, thereby maintaining this additional conduction path from the supply to ground.

When emerging from a shutdown condition, the charge stored in the capacitors on the high-pass filters can saturate the instrumentation amplifier and subsequent stages. The use of the fast restore feature helps reduce the recovery time and, therefore, minimize on time in power sensitive applications.

INPUT PROTECTION

All terminals of the AD8232 are protected against ESD. In addition, the input structure allows for dc overload conditions that are a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, use an external resistor in series with each of the inputs to limit current for voltages beyond the supplies. In either scenario, the AD8232 safely handles a continuous 5 mA current at room temperature.

For applications where the AD8232 encounters extreme overload voltages, such as in cardiac defibrillators, use external series resistors and gas discharge tubes (GDT). Neon lamps are commonly used as an inexpensive alternative to GDTs. These devices can handle the application of large voltages but do not maintain the voltage below the absolute maximum ratings for the AD8232. A complete solution includes further clamping to either supply using additional resistors and low leakage diode clamps, such as BAV199 or FJH1100.

As a safety measure, place a resistor between the input pin and the electrode that is connected to the subject to ensure that the current flow never exceeds 10 µA. Calculate the value of this resistor to be equal to the supply voltage across the AD8232 divided by 10 µA.

RADIO FREQUENCY INTERFERENCE (RFI)

Radio frequency (RF) rectification is often a problem in applications where there are large RF signals. The problem appears as a dc offset voltage at the output. The AD8232 has a 15 pF gate capacitance and 10 kΩ resistors at each input. This forms a low-pass filter on each input that reduces rectification at high frequency (see Figure 53) without the addition of external elements.

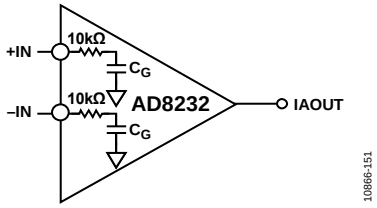


Figure 52. RFI Filter Without External Capacitors

For increased filtering, additional resistors can be added in series with each input. They must be placed as close as possible to the instrumentation amplifier inputs. These can be the same resistors used for overload and patient protection.

POWER SUPPLY REGULATION AND BYPASSING

The AD8232 is designed to be powered directly from a single 3 V battery, such as CR2032 type. It can also operate from rechargeable lithium-ion batteries, but the designer must take into account that the voltage during a charge cycle may exceed the absolute maximum ratings of the AD8232. To avoid damage to the part, use a power switch or a low power, low dropout regulator, such as ADP150.

In addition, excessive noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the chip power supplies. Place a 0.1 µF capacitor close to the supply pin. A 1 µF capacitor can be used farther away from the part. In most cases, the capacitor can be shared by other integrated circuits. Keep in mind that excessive decoupling capacitance increases power dissipation during power cycling.

INPUT REFERRED OFFSETS

Because of its internal architecture, the instrumentation amplifier should be used always with the DC blocking amplifier, shown as HPA in Figure 45.

As described in the Theory of Operation section, the dc blocking amplifier attenuates the input referred offsets present at the inputs of the instrumentation amplifier. However, this is true only when the dc blocking amplifier is used as an integrator. In this configuration, the input offsets from the dc blocking amplifier dominate appear directly at the output of the instrumentation amplifier.

If the dc blocking amplifier is used as a follower instead of its intended function as an integrator, the input referred offsets of the in-amp are amplified by a factor of 100.

LAYOUT RECOMMENDATIONS

It is important to follow good layout practices to optimize system performance. In low power applications, most resistors are of a high value to minimize additional supply current. The challenge of using high value resistors is that high impedance nodes become even more susceptible to noise pickup and board parasitics, such as capacitance and surface leakages. Keep all of the connections between high impedance nodes as short as possible to avoid introducing additional noise and errors from corrupting the signal.

To maintain high CMRR over frequency, keep the input traces symmetrical and length matched. Place safety and input bias resistors in the same position relative to each input. In addition, the use of a ground plane significantly improves the noise rejection of the system.

APPLICATIONS INFORMATION

ELIMINATING ELECTRODE OFFSETS

The instrumentation amplifier in the AD8232 is designed to apply gain and to filter out near dc signals simultaneously. This capability allows it to amplify a small ECG signal by a factor of 100 yet reject electrode offsets as large as ±300 mV.

To achieve offset rejection, connect an RC network between the output of the instrumentation amplifier, HPSENSE, and HPDRIVE, as shown in Figure 53.

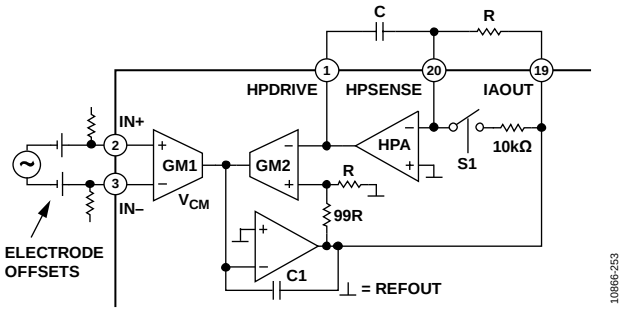


Figure 53. Eliminating Electrode Offsets

This RC network forms an integrator that feeds any near dc signals back into the instrumentation amplifier, thus eliminating the offsets without saturating any node and maintaining high signal gain.

In addition to blocking offsets present across the inputs of the instrumentation amplifier, this integrator also works as a high-pass filter that minimizes the effect of slow moving signals, such as baseline wander. The cutoff frequency of the filter is given by the equation

$$f_{-3dB} = \frac{100}{2\pi RC}$$

where *R* is in ohms and C is in farads.

Note that the filter cutoff is 100 times higher than is typically expected from a single-pole filter. Because of the feedback architecture of the instrumentation amplifier, the typical filter cutoff equation is modified by the gain of 100 of the instrumentation amplifier.

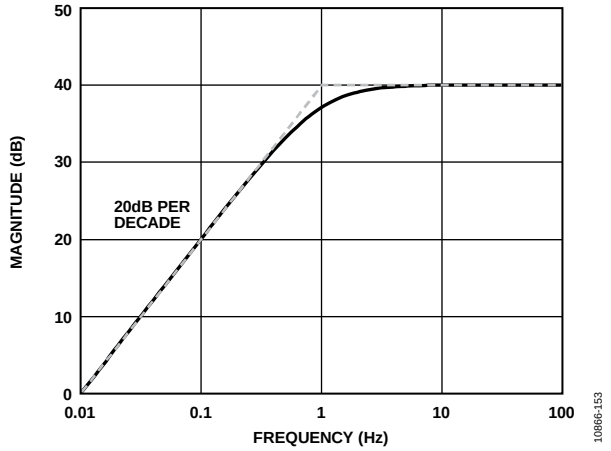


Figure 54. Frequency Response of Single-Pole DC Blocking Circuit

Just like with any high-pass filter with low frequency cutoff, any fast change in dc offset takes a long time to settle. If such change saturates the instrumentation amplifier output, the S1 switch briefly enables the 10 kΩ resistor path, thus moving the cutoff frequency to

$$f_{-3dB} = \frac{100(R+10^4)}{2\pi RC(10^4)} \quad (1)$$

For values of R greater than 100 kΩ, the expression in Equation 1 can be approximated by

$$f_{-3dB} = \frac{1}{200\pi C}$$

This higher cutoff reduces the settling time and enables faster recovery of the ECG signal. For more information, see the Fast Restore Circuit section.

HIGH-PASS FILTERING

The AD8232 can implement higher order high-pass filters. A higher filter order yields better artifact rejection but at a cost of increased signal distortion and more passive components on the printed circuit board (PCB).

Two-Pole High-Pass Filter

A two-pole architecture can be implemented by adding a simple ac coupling RC at the output of the instrumentation amplifier, as shown in Figure 55.

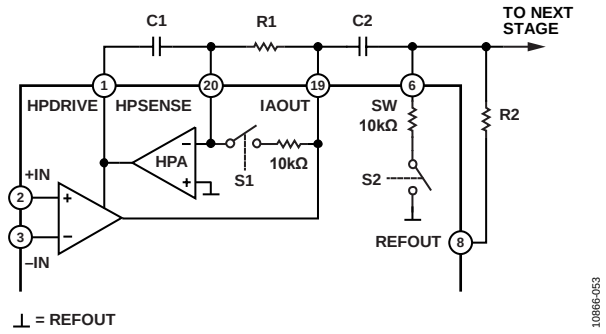


Figure 55. Schematic for a Two-Pole High-Pass Filter

Note that the right side of C2 connects to the SW terminal. Just like S1, S2 reduces the recovery time for this ac coupling network by placing 10 kΩ in parallel with R2. See the Fast Restore Circuit section for additional details on switch timing and trigger conditions.

Keep in mind that if this passive network is not buffered, it exhibits higher output impedance at the input of a subsequent low-pass filter, such as with Sallen-Key filter topologies. Careful component selection can yield good results without a buffer. See the Low-Pass Filtering and Gain section for additional information on component selection.

Additional High-Pass Filtering Options

In addition to the topologies explained in the previous sections, an additional pole may be added to the dc blocking circuit for additional rejection of low frequency signals. This configuration is shown in Figure 56.

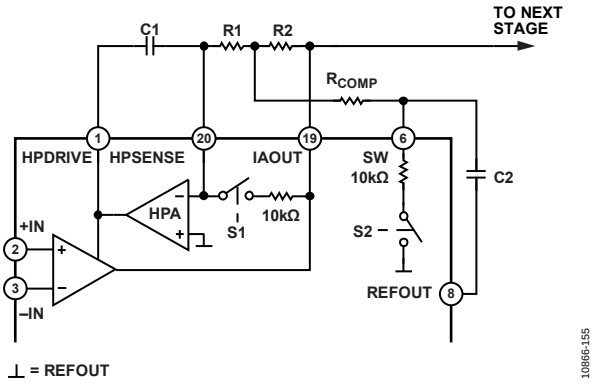


Figure 56. Schematic for an Alternative Two-Pole High-Pass Filter

An extra benefit of this circuit topology is that it allows lower cutoff frequency with lower R and C values and the resistor, R_{COMP}, can be used to control the Q of the filter to achieve narrow band-pass filters (for heart rate detection) or maximum pass-band flatness (for cardiac monitoring).

With this topology, the filter attenuation reverts to a single pole roll off at very low frequencies. Because the initial roll off was 40 dB per decade, this reversion to 20 dB per decade has little impact on the ability of the filter to reject out-of-band low frequency signals.

The designer may choose different values to achieve the desired filter performance. To simplify the design process, use the following recommendations as a starting point for component value selection.

$$R1 = R2 \geq 100\ k\Omega$$

$$C1 = C2$$

$$R_{COMP} = 0.14 \times R1$$

The cutoff frequency is located at

$$f_C = \frac{10}{2\pi\sqrt{R1\ C1\ R2\ C2}}$$

The selection of R_{COMP} to be 0.14 times the value of the other two resistors optimizes the filter for a maximally flat pass band. Reduce its value to increase the Q and, consequently, the peaking of the filter. Keep in mind that a very low value of R_{COMP} can result in an unstable circuit. The selection of values based on these criteria result in a transfer function similar to the one shown in Figure 58.

When additional low frequency rejection is desired, a high-order high-pass filter can be implemented by adding an ac coupling network at the output of the instrumentation amplifier, as shown in Figure 57. The SW terminal is connected to the ac coupling network to obtain the best settling time response when fast restore engages.

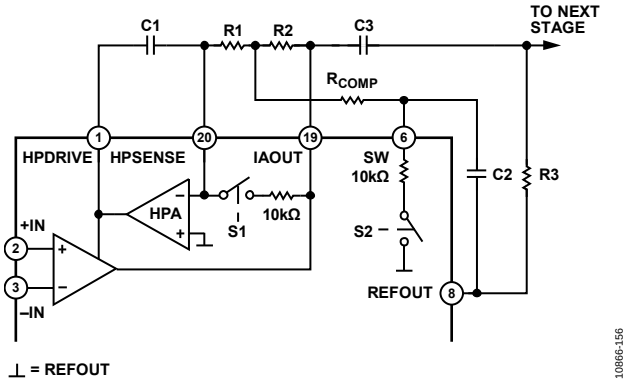


Figure 57. Schematic for a Three-Pole High-Pass Filter

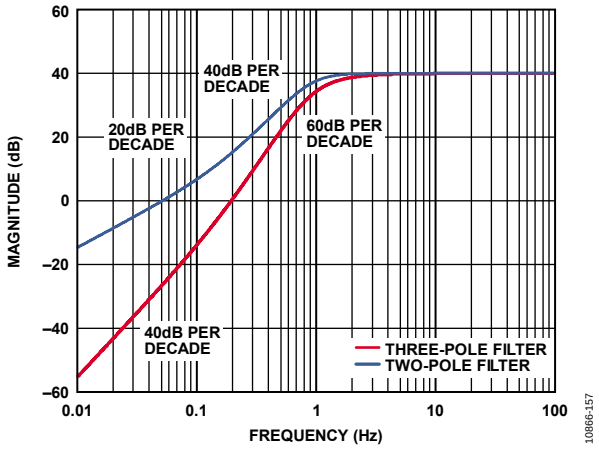


Figure 58. Frequency Response of Circuits in Figure 56 and Figure 57

Careful analysis and adjustment of all of the component values in practice is recommended to optimize the filter characteristics. A useful hint is to reduce the value of R_{COMP} to increase the peaking of the active filter to overcome the additional roll off introduced by the ac coupling network. Proper adjustment can yield the best pass-band flatness.

The design of the high-pass filter involves tradeoffs between signal distortion, component count, low frequency rejection, and component sizes. For example, a single-pole high-pass filter results in the least distortion to the signal, but its rejection of low-frequency artifacts is the lowest Table 4 compares the recommended filtering options.

Table 4. Comparison of High-Pass Filtering Options

	Filter Order	Component Count	Low Frequency Rejection	Capacitor Sizes/Values	Signal Distortion[1]	Output Impedance[2]
Figure 53	1	2	Good	Large	Low	Low
Figure 55	2	4	Better	Large	Medium	Higher
Figure 56	2	5	Better	Smaller	Medium	Low
Figure 57	3	7	Best	Smaller	Highest	Higher

[1] For equivalent corner frequency location.
[2] Output impedance refers to the drive capability of the high-pass filter before the low-pass filter. Low output impedance is desirable to allow flexibility in the selection of values for a low-pass filter, as explained in the Low-Pass Filtering and Gain section.

LOW-PASS FILTERING AND GAIN

The AD8232 includes an uncommitted op amp that can be used for extra gain and filtering. For applications that do not require a high-order filter, a simple RC low-pass filter should suffice, and the op amp can buffer or further amplify the signal.

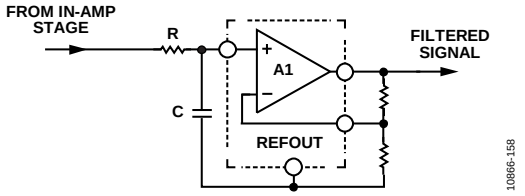


Figure 59. Schematic for a Single-Pole Low-Pass Filter and Additional Gain

Applications that require a steeper roll off or a sharper cut off, a Sallen-Key filter topology can be implemented, as shown in Figure 60.

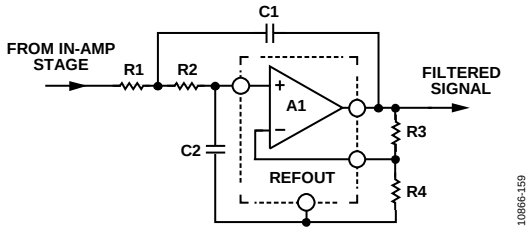


Figure 60. Schematic for a Two-Pole Low-Pass Filter

The following equations describe the low-pass cut off frequency, gain, and Q:

$$f_C = 1/(2\pi\sqrt{(R1\ C1\ R2\ C2)})$$

$$Gain = 1 + R3/R4$$

$$Q = \frac{\sqrt{R1 \times C1 \times R2 \times C2}}{R1 \times C2 + R2 \times C2 + R1 \times C1(1 - Gain)}$$

Note that changing the gain has an effect on Q and vice versa. Common values for Q are 0.5 to avoid peaking or 0.7 for maximum flatness and sharp cut off. A high value of Q can be used in narrow-band applications to increase peaking and the selectivity of the band-pass filter.

A common design procedure is to set R1 = R2 = R and C1 = C2 = C, which simplifies the expressions for cutoff frequency and Q to

$$f_C = 1/(2\pi RC)$$

$$Q = \frac{1}{3 - Gain}$$

Note that Q can be controlled by setting the gain with R3 and R4; however, this limits the gain to be less than 3. For gain values equal to or greater than 3, the circuit becomes unstable. A simple modification that allows higher gains is to make the value of C2 at least four times larger than C1.

It is important to note that these design equations only hold true in the case that the output impedance of the previous stage is much lower than the input impedance of the Sallen-Key filter. This is not the case when using an ac coupling network between the instrumentation amplifier output and the input of the low-pass filter without a buffer.

To connect these two filtering stages properly without a buffer, make the value of R1 at least ten times larger than the resistor of the ac coupling network (labeled as R2 in Figure 55).

DRIVING ANALOG-TO-DIGITAL CONVERTERS

The ability of AD8232 to drive capacitive loads makes it ideal to drive an ADC without the need for an additional buffer. However, depending on the input architecture of the ADC, a simple low-pass RC network may be required to decouple the transients from the switched-capacitor input typical of modern ADCs. This RC network also acts as an additional filter that can help reduce noise and aliasing. Follow the recommended guidelines from the ADC data sheet for the selection of proper R and C values.

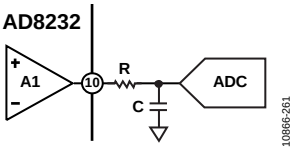


Figure 61. Driving an ADC

DRIVEN ELECTRODE

A driven lead (or reference electrode) is often used to minimize the effects of common-mode voltages induced by the power line and other interfering sources. The AD8232 extracts the common-mode voltage from the instrumentation amplifier inputs and makes it available through the RLD amplifier to drive an opposing signal into the patient. This functionality maintains the voltage between the patient and the AD8232 at a near constant, greatly improving the common-mode rejection ratio.

As a safety measure, place a resistor between the RLD pin and the electrode connected to the subject to ensure that current flow never exceeds 10 μA. Calculate the value of this resistor to be equal to the supply voltage across the AD8232 divided by 10 μA.

The AD8232 implements an integrator formed by an internal 150 kΩ resistor and an external capacitor to drive this electrode. Choice of the integrator capacitor is a tradeoff between line rejection capability and stability. The capacitor should be small to maintain as much loop gain as possible, around 50 Hz and 60 Hz, which are typical line frequencies. For stability, the gain of the integrator should be less than unity at the frequency of any other poles in the loop, such as those formed by the patient's capacitance and the safety resistors. The suggested application circuits use a 1 nF capacitor, which results in a loop gain of about 20 at line frequencies, with a crossover frequency of about 1 kHz.

In a two-lead configuration, the RLD amplifier can be used to drive the bias current resistors on the inputs. Although not as effective as a true driven electrode, this configuration can provide some common-mode rejection improvement if the sense electrode impedance is small and well matched.

APPLICATION CIRCUITS

HEART RATE MEASUREMENT NEXT TO THE HEART

For wearable exercise devices, the AD8232 is typically placed in a pod near the heart. The two sense electrodes are placed underneath the pectoral muscles; no driven electrode is used. Because the distance from the heart to the AD8232 is small, the heart signal is strong and there is less muscle artifact interference.

In this configuration, space is at a premium. By using as few external components as possible, the circuit in Figure 62 is optimized for size.

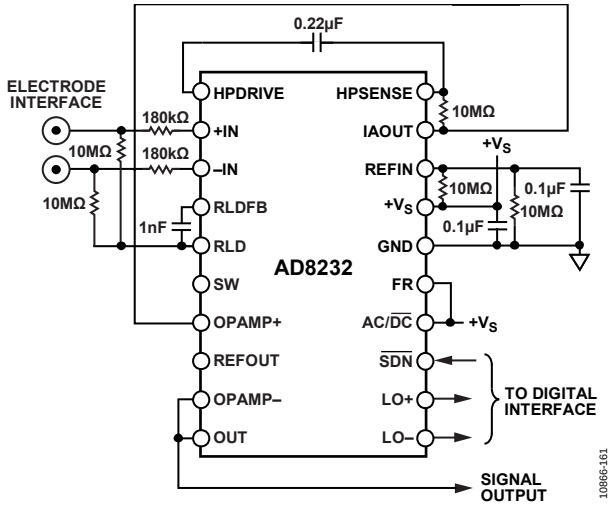


Figure 62. Circuit for Heart Rate Measurement Next to Heart

A shorter distance from the AD8232 to the heart makes this application less vulnerable to common-mode interference. However, since RLD is not used to drive an electrode, it can be used to improve the common-mode rejection by maintaining the midscale voltage through the 10 MΩ bias resistors.

A single-pole high-pass filter is set at 7 Hz, and there is no low-pass filter. No gain is used on the output op amp thereby reducing the number of resistors for a total system gain of 100.

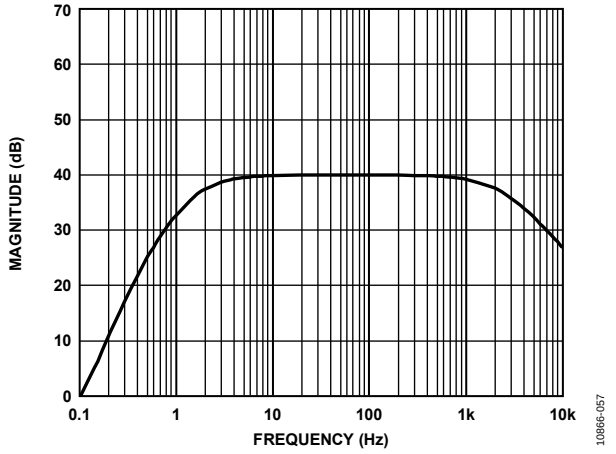


Figure 63. Frequency Response for HRM Next to Heart Circuit

The input terminals in this configuration use two 180 kΩ resistors, to protect the user from fault conditions. Two 10 MΩ resistors provide input bias. Use higher values for electrodes with high output impedance, such as cloth electrodes.

The schematic also shows two 10 MΩ resistors to set the midscale reference voltage. If there is already a reference voltage available, it can be driven into the REFIN input to eliminate these two 10 MΩ resistors.

EXERCISE APPLICATION: HEART RATE MEASURED AT THE HANDS

In this application, the heart rate signal is measured at the hands with stainless steel electrodes. The user's arm and upper body movement create large motion artifacts and the long lead length makes the system susceptible to common-mode interference. A very narrow band-pass characteristic is required to separate the heart signal from the interferers.

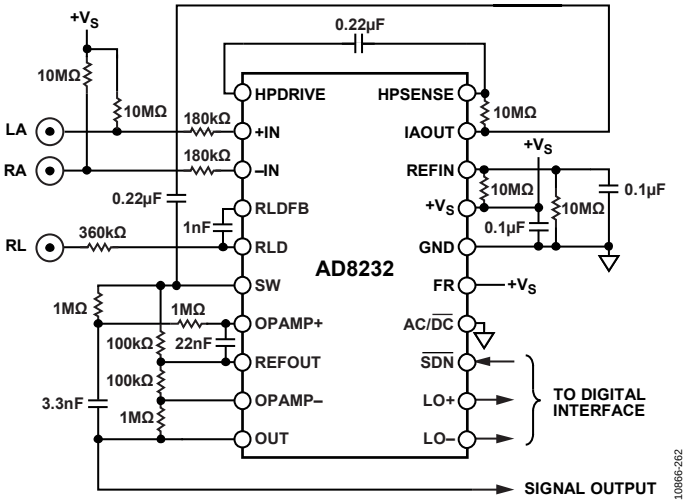


Figure 64. Circuit for Heart Rate Measurement at Hands

The circuit in Figure 64 uses a two-pole high-pass filter set at 7 Hz. A two-pole low-pass filter at 24 Hz follows the high-pass filters to eliminate any other artifacts and line noise.

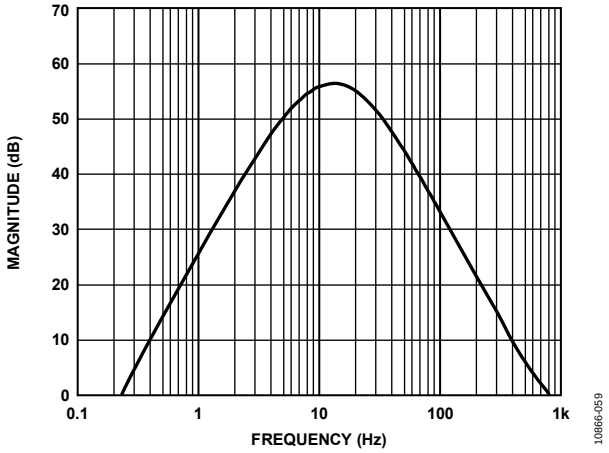


Figure 65. Frequency Response for HRM Circuit Taken at the Hands

The overall narrow-band nature of this filter combination distorts the ECG waveform significantly. Therefore, it is only suitable to determine the heart rate, and not to analyze the ECG signal characteristics.

The low-pass filter stage also includes a gain of 11, to bring the total system gain close to 1100 (note that the filter roll off prevents the maximum gain from reaching this value). Because the ECG signal is measured at the hands, it is weaker than when measured closer to the heart.

The RLD circuit drives to the third electrode, which can also be located at the hands, to cancel common-mode interference.

CARDIAC MONITOR CONFIGURATION

This configuration is designed for monitoring the shape of the ECG waveform. It assumes that the patient remains relatively still during the measurement, and therefore, motion artifacts are less of an issue.

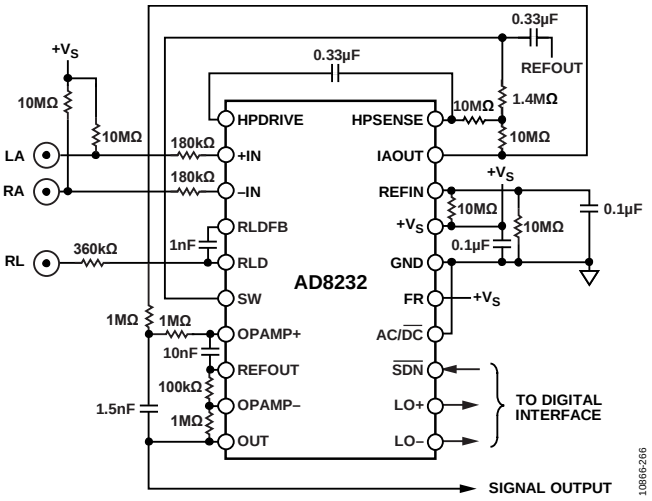


Figure 66. Circuit for ECG Waveform Monitoring

To obtain an ECG waveform with minimal distortion, the AD8232 is configured with a 0.5 Hz two-pole high-pass filter followed by a two-pole, 40 Hz, low-pass filter. A third electrode is driven for optimum common-mode rejection.

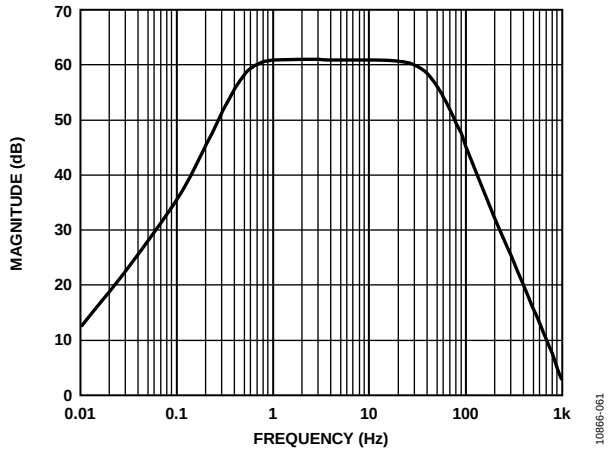


Figure 67. Frequency Response of Cardiac Monitor Circuit

In addition to 40 Hz filtering, the op amp stage is configured for a gain of 11, resulting in a total system gain of 1100. To optimize the dynamic range of the system, the gain level is adjustable, depending on the input signal amplitude (which may vary with electrode placement) and ADC input range.

PORTABLE CARDIAC MONITOR WITH ELIMINATION OF MOTION ARTIFACTS

The circuit in Figure 68 shows an implementation of a battery-powered embedded system for monitoring heart rate in applications where the patient engages in moderate activity, such as with a Holter monitor. The AD8232 uses a three-electrode patient interface and implements a two-pole high-pass filter with a cutoff at 0.3 Hz, and a two-pole low-pass filter with a cutoff frequency of 37 Hz. The total signal gain in the pass band is 400. The fully conditioned signal is sampled by the sigma-delta ADC integrated on the low power microcontroller, ADuCM360. The wide dynamic range of this ADC provides flexibility to reduce the signal gain to avoid saturation, depending on electrode placement.

Because the pass band is relatively wide for ambulatory applications, the ADXL346 accelerometer signal can be used to further minimize the noise introduced by the motion of the patient. Moreover, the microcontroller can use the motion information to monitor inactivity and to issue a system shutdown to save battery power.

The low dropout regulator ensures that the maximum of 3 V is not exceeded, especially during charge cycles of the battery, which can be a lithium-ion cell.

In this application, the ADuCM360 uses its Port 0 to perform DMA transfers to the host communication interface or to an on-board memory, if recording the waveform for later transfer. However, in any particular application, this port should be used for the busiest interface to minimize CPU cycles and maintain low power operation.

Note that this circuit is shown to demonstrate the capabilities of AD8232 and other system components. It is not a complete system design and additional effort must be made to ensure compliance with medical safety guidelines from regulatory agencies.

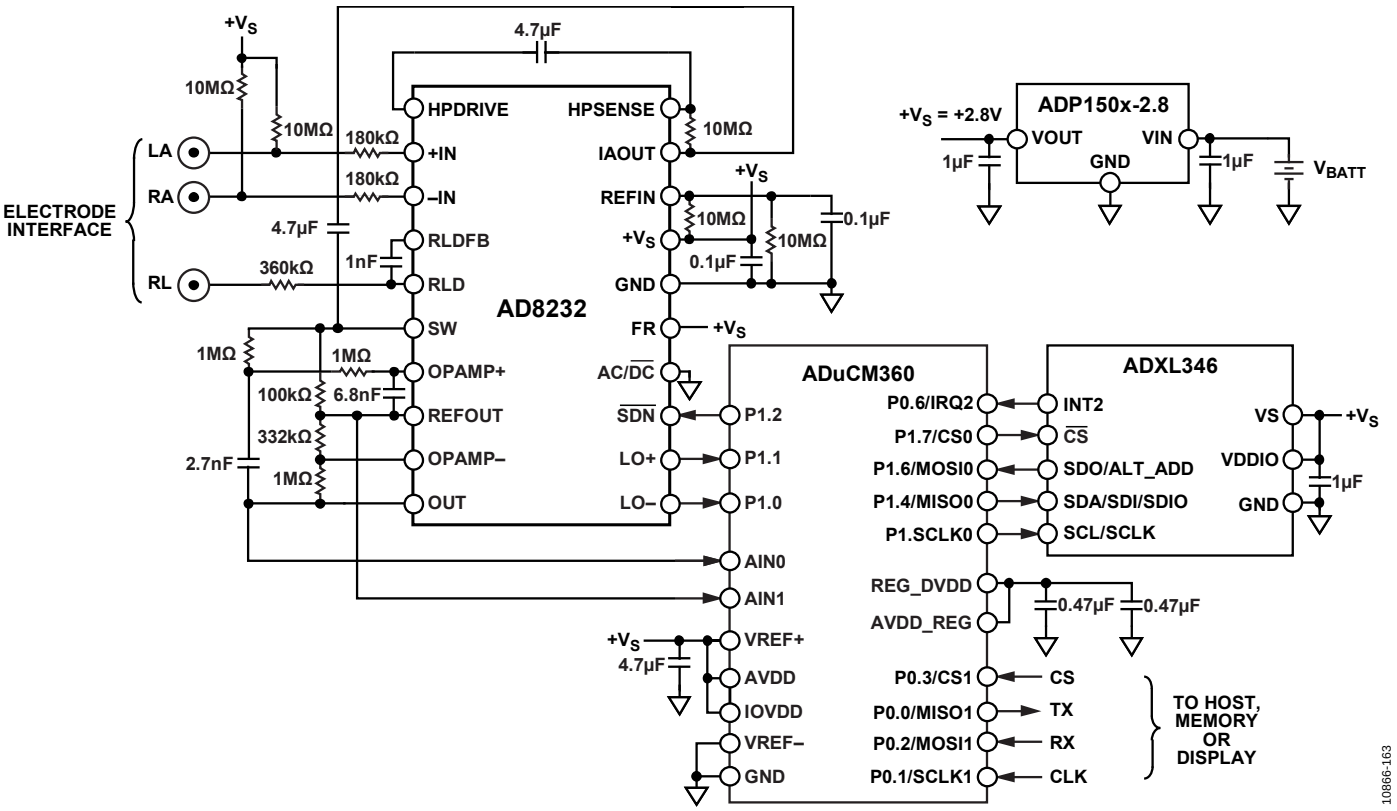
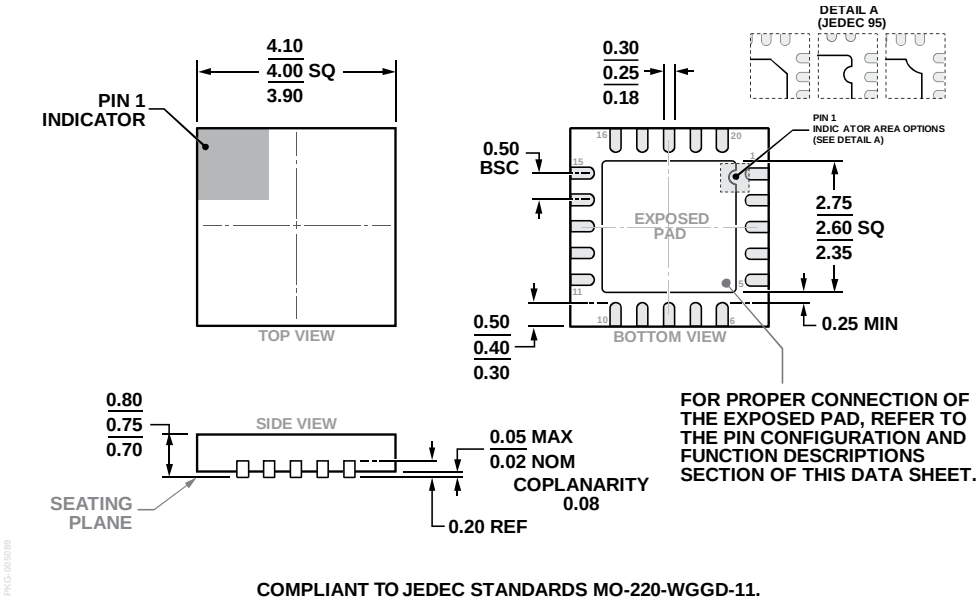


Figure 68. Low Power Portable Cardiac Monitor

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 69. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8232ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD8232ACPZ-RL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD8232ACPZ-WP	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD8232-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

LM741 Operational Amplifier

1 Features

- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

- Comparators
- Multivibrators
- DC Amplifiers
- Summing Amplifiers
- Integrator or Differentiators
- Active Filters

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common-mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741 and LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM741	TO-99 (8)	9.08 mm × 9.08 mm
	CDIP (8)	10.16 mm × 6.502 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

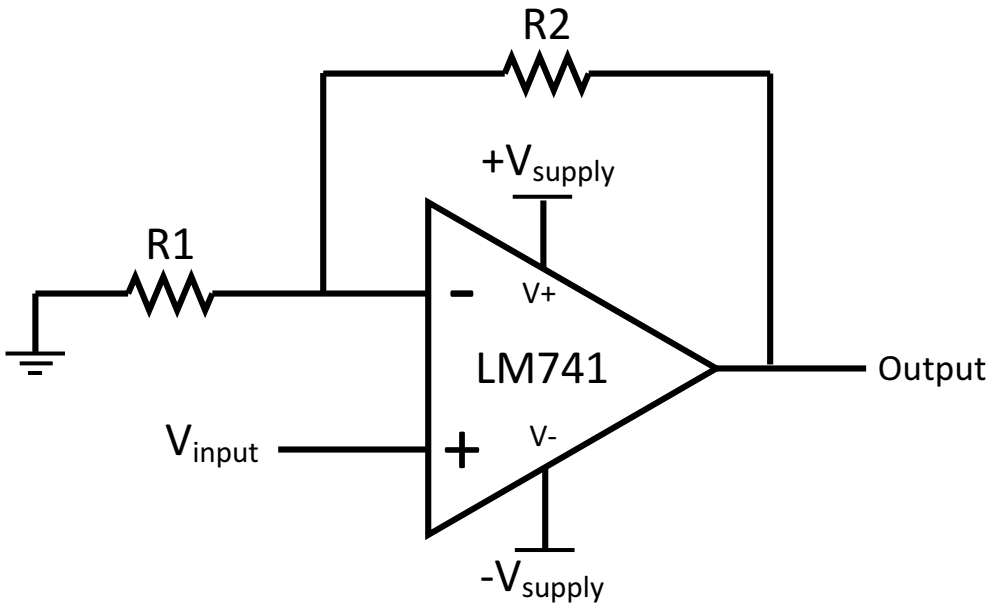


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2004) to Revision D **Page**

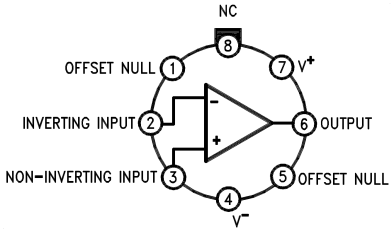
- Added *Applications* section, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed NAD 10-Pin CLGA pinout ... 3
- Removed obselete M (S0-8) package from the data sheet ... 4
- Added recommended operating supply voltage spec ... 4
- Added recommended operating temperature spec ... 4

Changes from Revision C (March 2013) to Revision D **Page**

- Added *Applications* section, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed NAD 10-Pin CLGA pinout ... 3
- Removed obselete M (S0-8) package from the data sheet ... 4
- Added recommended operating supply voltage spec ... 4
- Added recommended operating temperature spec ... 4

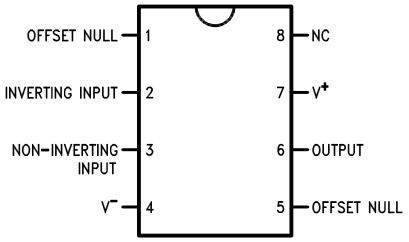
5 Pin Configuration and Functions

LMC Package
8-Pin TO-99
Top View



LM741H is available per JM38510/10101

NAB Package
8-Pin CDIP or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INVERTING INPUT	2	I	Inverting signal input
NC	8	N/A	No Connect, should be left floating
NONINVERTING INPUT	3	I	Noninverting signal input
OFFSET NULL	1, 5	I	Offset null pin used to eliminate the offset voltage and balance the input voltages.
OFFSET NULL			
OUTPUT	6	O	Amplified signal output
V+	7	I	Positive supply voltage
V–	4	I	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

		MIN	MAX	UNIT
Supply voltage	LM741, LM741A		±22	V
	LM741C		±18	
Power dissipation [4]			500	mW
Differential input voltage			±30	V
Input voltage [5]			±15	V
Output short circuit duration		Continuous		
Operating temperature	LM741, LM741A	–50	125	°C
	LM741C	0	70	
Junction temperature	LM741, LM741A		150	°C
	LM741C		100	
Soldering information	PDIP package (10 seconds)		260	°C
	CDIP or TO-99 package (10 seconds)		300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For military specifications see RETS741X for LM741 and RETS741AX for LM741A.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.
(5) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±400	V

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (VDD-GND)	LM741, LM741A	±10	±15	±22	V
	LM741C	±10	±15	±18	
Temperature	LM741, LM741A	–55		125	°C
	LM741C	0		70	

6.4 Thermal Information

THERMAL METRIC[1]		LM741			UNIT
		LMC (TO-99)	NAB (CDIP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170	100	100	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, LM741 (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage		$R_S \le 10\ k\Omega$	$T_A = 25°C$		1	5	mV
			$T_{AMIN} \le T_A \le T_{AMAX}$			6	mV
Input offset voltage adjustment range		$T_A = 25°C$, $V_S = \pm 20$ V			±15		mV
Input offset current		$T_A = 25°C$			20	200	nA
		$T_{AMIN} \le T_A \le T_{AMAX}$			85	500	
Input bias current		$T_A = 25°C$			80	500	nA
		$T_{AMIN} \le T_A \le T_{AMAX}$				1.5	µA
Input resistance		$T_A = 25°C$, $V_S = \pm 20$ V		0.3	2		MΩ
Input voltage range		$T_{AMIN} \le T_A \le T_{AMAX}$		±12	±13		V
Large signal voltage gain		$V_S = \pm 15$ V, $V_O = \pm 10$ V, $R_L \ge 2$ kΩ	$T_A = 25°C$	50	200		V/mV
			$T_{AMIN} \le T_A \le T_{AMAX}$	25			
Output voltage swing		$V_S = \pm 15$ V	$R_L \ge 10$ kΩ	±12	±14		V
			$R_L \ge 2$ kΩ	±10	±13		
Output short circuit current		$T_A = 25°C$			25		mA
Common-mode rejection ratio		$R_S \le 10\ \Omega$, $V_{CM} = \pm 12$ V, $T_{AMIN} \le T_A \le T_{AMAX}$		80	95		dB
Supply voltage rejection ratio		$V_S = \pm 20$ V to $V_S = \pm 5$ V, $R_S \le 10\ \Omega$, $T_{AMIN} \le T_A \le T_{AMAX}$		86	96		dB
Transient response	Rise time	$T_A = 25°C$, unity gain			0.3		µs
	Overshoot				5%		
Slew rate		$T_A = 25°C$, unity gain			0.5		V/µs
Supply current		$T_A = 25°C$			1.7	2.8	mA
Power consumption		$V_S = \pm 15$ V	$T_A = 25°C$		50	85	mW
			$T_A = T_{AMIN}$		60	100	
			$T_A = T_{AMAX}$		45	75	

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15$ V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

6.6 Electrical Characteristics, LM741A (1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \le 50\ \Omega$	$T_A = 25°C$		0.8	3	mV
		$T_{AMIN} \le T_A \le T_{AMAX}$			4	mV
Average input offset voltage drift					15	µV/°C
Input offset voltage adjustment range	$T_A = 25°C$, $V_S = \pm 20$ V		±10			mV
Input offset current	$T_A = 25°C$			3	30	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$				70	
Average input offset current drift					0.5	nA/°C
Input bias current	$T_A = 25°C$			30	80	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$				0.21	µA
Input resistance	$T_A = 25°C$, $V_S = \pm 20$ V		1	6		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20$ V		0.5			
Large signal voltage gain	$V_S = \pm 20$ V, $V_O = \pm 15$ V, $R_L \ge 2$ kΩ	$T_A = 25°C$	50			V/mV
		$T_{AMIN} \le T_A \le T_{AMAX}$	32			
	$V_S = \pm 5$ V, $V_O = \pm 2$ V, $R_L \ge 2$ kΩ, $T_{AMIN} \le T_A \le T_{AMAX}$		10			

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15$ V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

Electrical Characteristics, LM741A[1] (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage swing		V_S = ±20 V	R_L ≥ 10 kΩ	±16			V
			R_L ≥ 2 kΩ	±15			
Output short circuit current		T_A = 25°C		10	25	35	mA
		$T_{AMIN} \le T_A \le T_{AMAX}$		10		40	
Common-mode rejection ratio		R_S ≤ 50 Ω, V_{CM} = ±12 V, $T_{AMIN} \le T_A \le T_{AMAX}$		80	95		dB
Supply voltage rejection ratio		V_S = ±20 V to V_S = ±5 V, R_S ≤ 50 Ω, $T_{AMIN} \le T_A \le T_{AMAX}$		86	96		dB
Transient response	Rise time	T_A = 25°C, unity gain			0.25	0.8	µs
	Overshoot				6%	20%	
Bandwidth [2]		T_A = 25°C		0.437	1.5		MHz
Slew rate		T_A = 25°C, unity gain		0.3	0.7		V/µs
Power consumption		V_S = ±20 V	T_A = 25°C		80	150	mW
			$T_A = T_{AMIN}$			165	
			$T_A = T_{AMAX}$			135	

(2) Calculated value from: BW (MHz) = 0.35/Rise Time (µs).

6.7 Electrical Characteristics, LM741C[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage		R_S ≤ 10 kΩ	T_A = 25°C		2	6	mV
			$T_{AMIN} \le T_A \le T_{AMAX}$			7.5	mV
Input offset voltage adjustment range		T_A = 25°C, V_S = ±20 V			±15		mV
Input offset current		T_A = 25°C			20	200	nA
		$T_{AMIN} \le T_A \le T_{AMAX}$				300	
Input bias current		T_A = 25°C			80	500	nA
		$T_{AMIN} \le T_A \le T_{AMAX}$				0.8	µA
Input resistance		T_A = 25°C, V_S = ±20 V		0.3	2		MΩ
Input voltage range		T_A = 25°C		±12	±13		V
Large signal voltage gain		V_S = ±15 V, V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	20	200		V/mV
			$T_{AMIN} \le T_A \le T_{AMAX}$	15			
Output voltage swing		V_S = ±15 V	R_L ≥ 10 kΩ	±12	±14		V
			R_L ≥ 2 kΩ	±10	±13		
Output short circuit current		T_A = 25°C			25		mA
Common-mode rejection ratio		R_S ≤ 10 kΩ, V_{CM} = ±12 V, $T_{AMIN} \le T_A \le T_{AMAX}$		70	90		dB
Supply voltage rejection ratio		V_S = ±20 V to V_S = ±5 V, R_S ≤ 10 Ω, $T_{AMIN} \le T_A \le T_{AMAX}$		77	96		dB
Transient response	Rise time	T_A = 25°C, Unity Gain			0.3		µs
	Overshoot				5%		
Slew rate		T_A = 25°C, Unity Gain			0.5		V/µs
Supply current		T_A = 25°C			1.7	2.8	mA
Power consumption		V_S = ±15 V, T_A = 25°C			50	85	mW

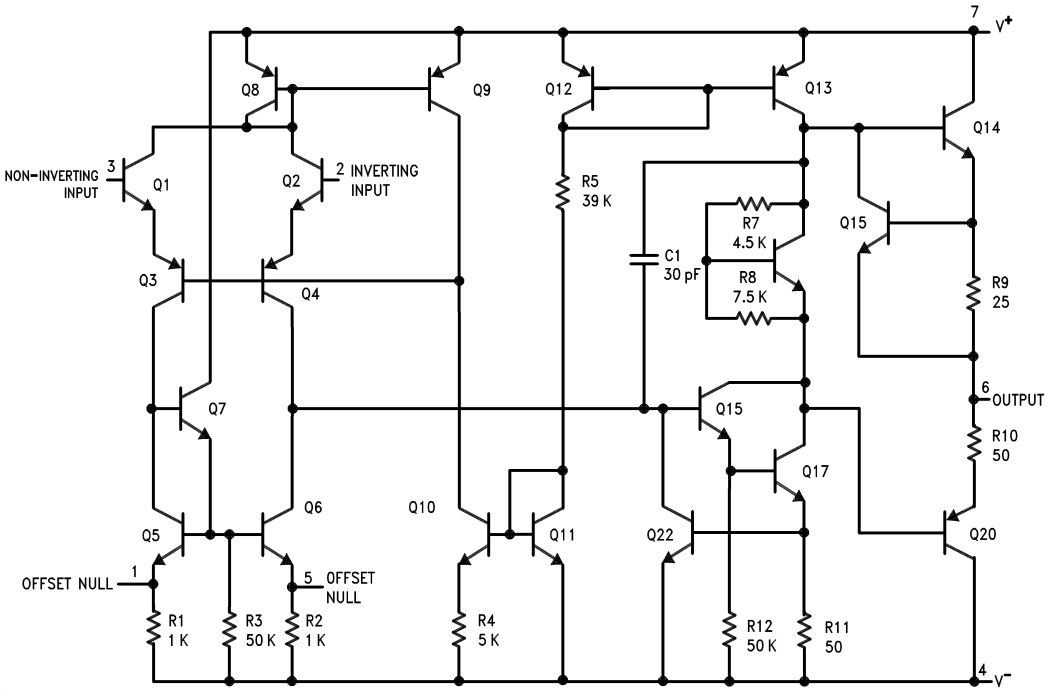
(1) Unless otherwise specified, these specifications apply for V_S = ±15 V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

7 Detailed Description

7.1 Overview

The LM74 devices are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications. The LM741 can operate with a single or dual power supply voltage. The LM741 devices are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overload Protection

The LM741 features overload protection circuitry on the input and output. This prevents possible circuit damage to the device.

7.3.2 Latch-up Prevention

The LM741 is designed so that there is no latch-up occurrence when the common-mode range is exceeded. This allows the device to function properly without having to power cycle the device.

7.3.3 Pin-to-Pin Capability

The LM741 is pin-to-pin direct replacements for the LM709C, LM201, MC1439, and LM748 in most applications. Direct replacement capabilities allows flexibility in design for replacing obsolete parts.

7.4 Device Functional Modes

7.4.1 Open-Loop Amplifier

The LM741 can be operated in an open-loop configuration. The magnitude of the open-loop gain is typically large thus for a small difference between the noninverting and inverting input terminals, the amplifier output will be driven near the supply voltage. Without negative feedback, the LM741 can act as a comparator. If the inverting input is held at 0 V, and the input voltage applied to the noninverting input is positive, the output will be positive. If the input voltage applied to the noninverting input is negative, the output will be negative.

7.4.2 Closed-Loop Amplifier

In a closed-loop configuration, negative feedback is used by applying a portion of the output voltage to the inverting input. Unlike the open-loop configuration, closed loop feedback reduces the gain of the circuit. The overall gain and response of the circuit is determined by the feedback network rather than the operational amplifier characteristics. The response of the operational amplifier circuit is characterized by the transfer function.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM741 is a general-purpose amplifier than can be used in a variety of applications and configurations. One common configuration is in a noninverting amplifier configuration. In this configuration, the output signal is in phase with the input (not inverted as in the inverting amplifier configuration), the input impedance of the amplifier is high, and the output impedance is low. The characteristics of the input and output impedance is beneficial for applications that require isolation between the input and output. No significant loading will occur from the previous stage before the amplifier. The gain of the system is set accordingly so the output signal is a factor larger than the input signal.

8.2 Typical Application

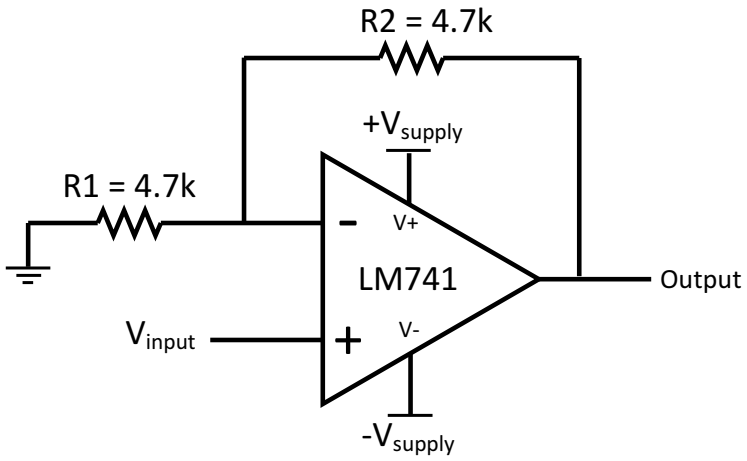


Figure 1. LM741 Noninverting Amplifier Circuit

8.2.1 Design Requirements

As shown in Figure 1, the signal is applied to the noninverting input of the LM741. The gain of the system is determined by the feedback resistor and input resistor connected to the inverting input. The gain can be calculated by Equation 1:

$$\text{Gain} = 1 + (R2/R1) \quad (1)$$

The gain is set to 2 for this application. R1 and R2 are 4.7-k resistors with 5% tolerance.

8.2.2 Detailed Design Procedure

The LM741 can be operated in either single supply or dual supply. This application is configured for dual supply with the supply rails at ±15 V. The input signal is connected to a function generator. A 1-Vpp, 10-kHz sine wave was used as the signal input. 5% tolerance resistors were used, but if the application requires an accurate gain response, use 1% tolerance resistors.

Typical Application (continued)

8.2.3 Application Curve

The waveforms in Figure 2 show the input and output signals of the LM741 non-inverting amplifier circuit. The blue waveform (top) shows the input signal, while the red waveform (bottom) shows the output signal. The input signal is 1.06 Vpp and the output signal is 1.94 Vpp. With the 4.7-kΩ resistors, the theoretical gain of the system is 2. Due to the 5% tolerance, the gain of the system including the tolerance is 1.992. The gain of the system when measured from the mean amplitude values on the oscilloscope was 1.83.

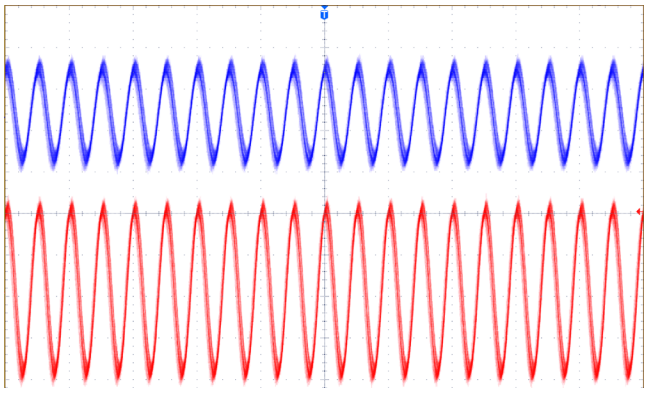


Figure 2. Waveforms for LM741 Noninverting Amplifier Circuit

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, a 0.1-µF capacitor is recommended and should be placed as close as possible to the LM741 power supply pins.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, take care with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize pick-up and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground. As shown in Figure 3, the feedback resistors and the decoupling capacitors are located close to the device to ensure maximum stability and noise performance of the system.

10.2 Layout Example

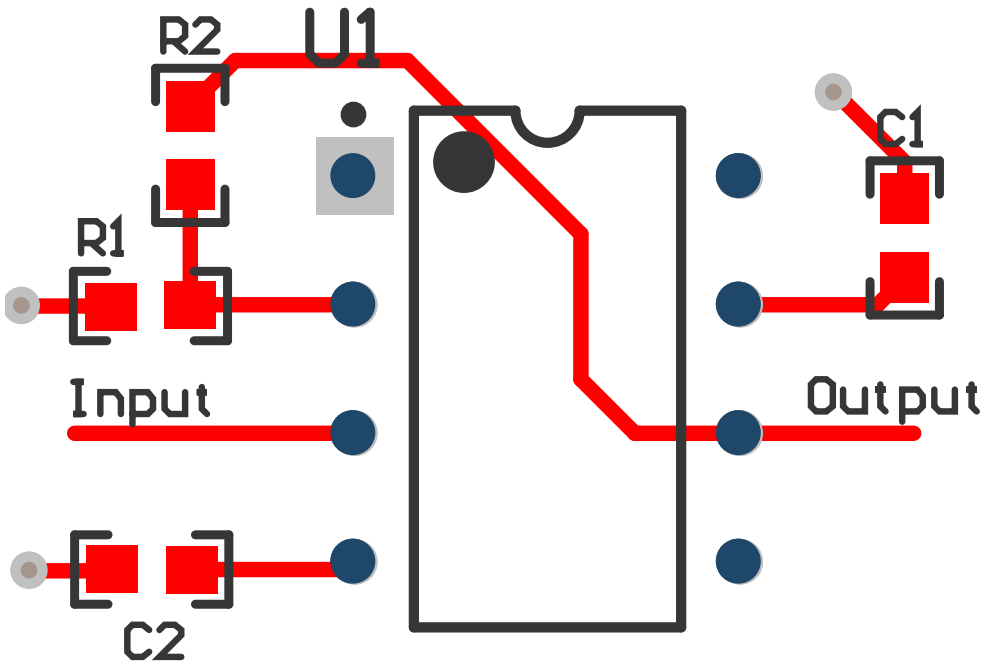


Figure 3. LM741 Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
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11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM741C-MWC	ACTIVE	WAFERSALE	YS	0	1	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LM741CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 741CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

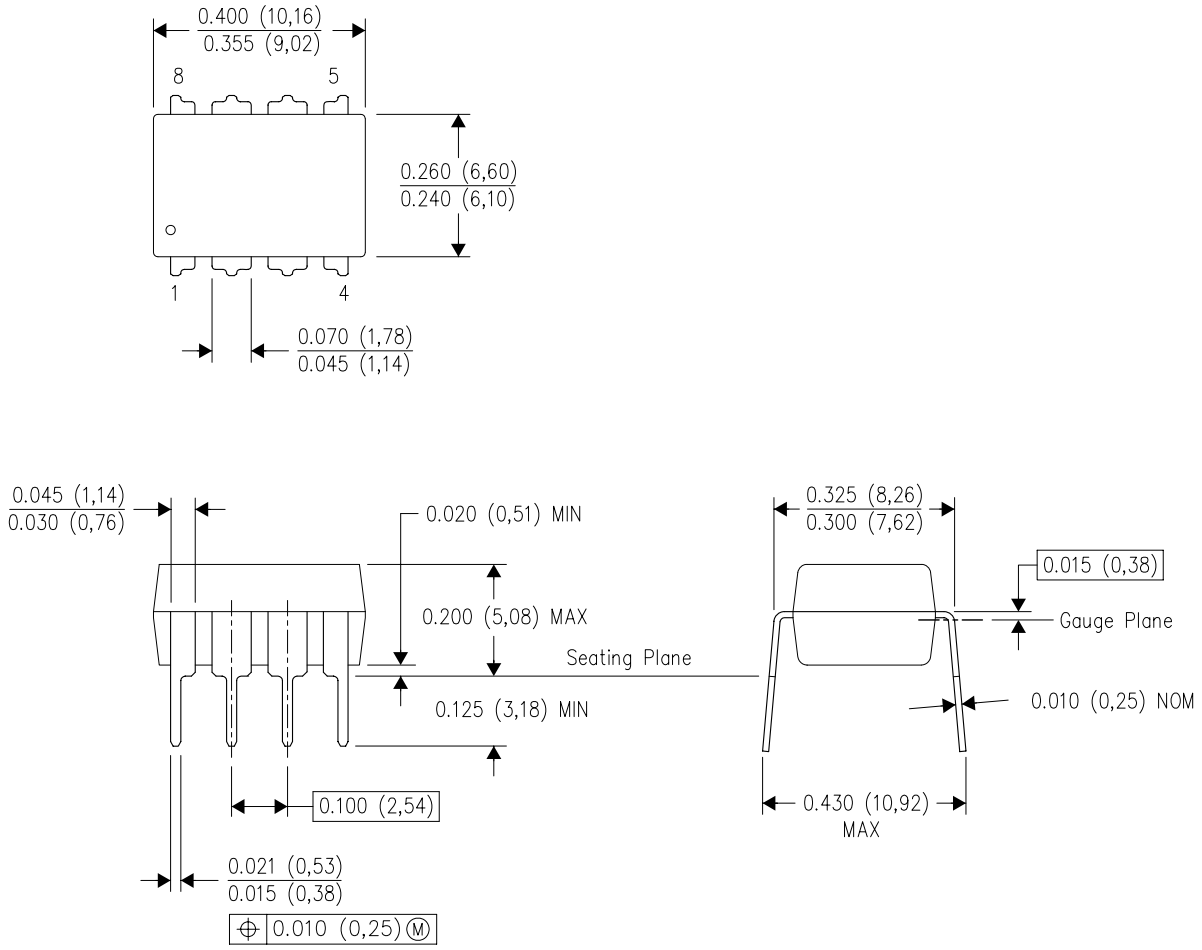
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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