DESIGN OF LOW 1/F NOISE OPERATIONAL AMPLIFIER CELL USING CHOPPER STABILIZATION TECHNIQUE

THESIS

MAGISTER PROGRAM OF ELECTRICAL ENGINEERING
CONCENTRATION CONTROL SYSTEM AND ELECTRONIC

Declared to obtain qualify
Master Degree in Engineering

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I dedicate this thesis to Mom and Dad.

Without their love and support,

I would never stay strong and keep moving when I broke down.

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ABSTRACT

Chopper stabilization technique can be widely employed for differential-input and differential-output amplifiers and can be implemented chopper switches back and forth of amplifiers. Actually, instrumentation amplifiers with chopper stabilization technique were designed and implemented in our laboratory. In this case, the chopper stabilization technique was employed for the first block only because the output of the second block is single ended form. Therefore, *1/f* noise generated in the second block could not be removed and was observed at the final output.

In this master thesis, the low *1/f* noise operational amplifier cell with differential-input and single-ended-output using chopper stabilization technique is presented. Especially, I focus on the symmetric property of the output cascade structure in the folded cascade operational amplifier, new chopper stabilization technique is applied to folded cascade based operational amplifier.

The proposed circuit was designed by Phenitec Semiconductor 3-Metal 0.6 µm CMOS process and evaluated by using HSPICE. According to the simulation results, I could confirm the proposed operational amplifier operates well. It has stable response (58.018º of phase margin) and high gain (126.56 dB). Moreover, *1/f* noise (as representation of inside noise of operational amplifier) can be separated with input signal, and then it is removed perfectly at the output node. Furthermore, the proposed circuit is applied into inverting amplifier circuit and instrumentation amplifier for its application examples. These circuits were also evaluated by HSPICE. I could confirm that the application circuits also operated well as theory.

CHAPTER I
INTRODUCTION

1.1 Background

Birthrate in each country around the world is greatly increasing every year. Some of countries suffer of low life expectancy. However, more than 40 years, life expectancy is estimated 25 years longer than 1900 era. This is the real proof of life expectancy increment. This happen because of medical and health care system development [1].

Electrooculogram (EOG), electroencephalogram (EEG), electrocardiogram (ECG), electromyogram (EMG) are widely used to operate medical and health care system. These are kinds of signal which are very weak and known as biological signals. The biological signals have a small amplitude and low frequency [2]. This condition is described by Figure 1, the range of most known biological signals are in the order of µV to mV and works on the order of Hz to a few kHz. This characteristics are expressed in detail in Figure 1 [3].

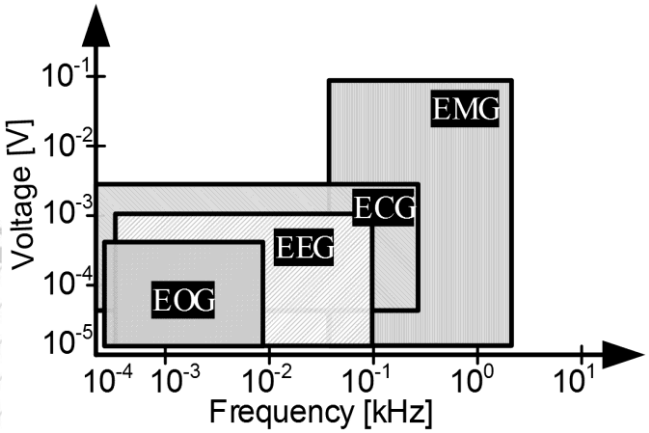

Figure 1. Characteristic of biological signals

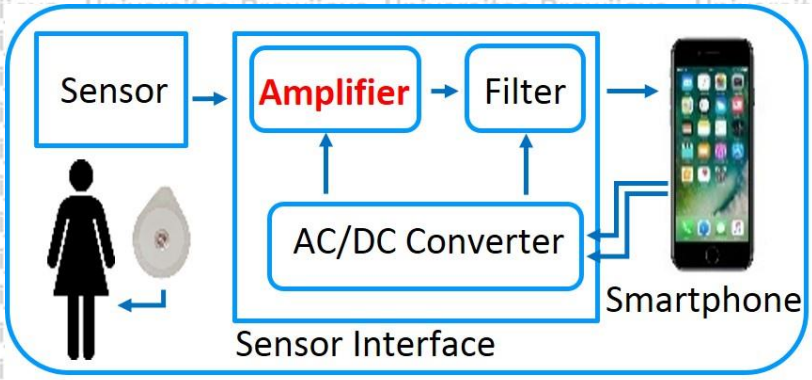

Figure 2. Block diagram of biological signal processing system

Figure 2 explains about block diagram of biological signal devices system. In this biological signal devices, biological signal is acquired by a pair of electrodes. Processing, recording and analyzing will come after that. The output of processing term (inside sensor interface block) will enter some devices to be recorded and analyzed [4]. This system is known as biological signal processing.

In spite of this system description and its extensive use, a lot of difficulties especially in practical term cannot be avoided[5].One of this problem occurs in amplifier of sensor interface block, (refers to Figure 2). As common knowledge, an amplifier has a lot of semiconductor devices inside, especially MOSFET transistor. Unfortunately, *1/f* noise or also known flicker noise or pink noise is spread over in MOSFET transistor [6]. In addition, *1/f* noise has a characteristic to dominate low frequencies and if the device size is reduced, its amount will increase [7]. Furthermore, it will show up randomly and made a limitation for information signal (biological signal), thus the signal is difficult to be detected. However, through *1/f* noise power spectral density distribution, *1/f* noise behavior can be predicted [8].

Such of biological signal condition (low frequency range and the characteristic of *1/f* noise) is emphasis if biological signal has to be amplified before it is analyzed. In addition, the used amplifier would be better if has the following characteristic: large voltage gains, stable in responses, and small noises. Noted, input sensor provide not only common mode DC offset but also common mode in 50 Hz or 60 Hz power transmission line [9]. This will give additional noises.

The example of this amplifier is Instrumentation Amplifier (IA) which consists of Fully Balanced Differential Difference Amplifier (FBDDA) and Differential Difference Amplifier (DDA) which are combined with Chopper Stabilization Technique (CST) [10]. However, in this circuit, CST was applied onto FBDDA only. Therefore, noises and offset in DDA was not reduced using this technique. Moreover, it is difficult to apply CST directly into operational amplifier with single-ended input. In order to overcome this problem, Design of Low *1/f* Noise Operational Amplifier Cell Using Chopper Stabilization Technique is proposed. In this thesis, CST is implemented into amplifier and packed as one Operational Amplifier Cell.

1.2 Objective

The objective of this master thesis is to design an operational amplifier which has differential input and single-ended output, with *1/f* noise reduction. In order to achieve this objective, Folded Cascode Operational Amplifier (FC Op-Amp) with new Chopper Stabilization Technique (CST) are employed.

1.3 Outline

The organization of this master thesis starts in Chapter 1. This chapter 1 is about a brief introduction of the master thesis which contains background of the research, objective and master thesis outline.

Chapter 2 explains of theoretical literatures. Several main points are mentioned in chapter 2, they are: basic of MOSFET transistor, Noises, Operational Amplifier and lastly Chopper Stabilization Technique.

Basic of MOSFET transistor devices is explained about MOS terminal pins, its physical conditions and the last is about its characteristics. In physical conditions, there will be described of design and fabrication of MOSFET transistor. Working region of MOSFET transistor is explained in MOSFET's characteristic. The current of MOSFET is influenced by bias voltage each terminal will be explained.

Following the prior explanation, noises are explained in next part. In the beginning of this explanation, this master thesis explains about noises in general. Next, this noises are focused on MOSFET's noise. It will be about its noise modeling and equations. Therefore, as addition, briefly it will be shown the equivalent circuit of noiseless operational amplifier and the noise equivalent place. *1/f* noise is one kind of special noise got more detailed in this master thesis such as its features, its connection with another noise, etc.

The literature of operational amplifier is written down next. Differential Amplifier (DA) and its equation derivation will be stated. Then, two stage operational amplifier is described. On the last point of chapter 2, Chopper Stabilization Technique (CST) is the main topic. In this part, the operations of CST are expressed.

Chapter 3 is written to unfold the basic idea of the proposed system. Before the proposed system described, a brief of IA and FBDDA-DDA will be explained. This will be focused on its responses, the reduction of offset and *1/f* noise, and the condition of DA for IA and DDA for FBDDA.

After that, operational amplifier cell is proposed in order to overcome this problem. Its component will be exposed one by one. Explanation is given in each part of it, such as the explanation about how the folded cascode works, its equations, then its connection to class AB common source (stands for second stage of operational amplifier) and its pole condition. The last part will be explained about CST relationship and its noise reduction.

Next chapter is written down to explain about analysis and discussion. In this chapter 4, simulation results of proposed system are shown and explained. The comparison result of IA (as representation and simple circuit of FBDDA-DDA) and the proposed system will be analyzed.

The last is chapter 5. It contains the conclusion and the recommendation for future work in respect to this master thesis.

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CHAPTER II
THEORETICAL LITERATURE

2.1 MOS Devices and Characteristic

Metal Oxide Semiconductor Integrated Circuit (MOS IC) is one of several semiconductors in the world. MOS consist of two type, PMOS and NMOS. Both of them are complement of each other and has four pins or four terminals. These pins are Gate, Source, Drain and Back-Gate/Bulk. The back-gate for PMOS connects to VDD and NMOS case, it connects to VSS. This connection is shown in Figure 3[11].

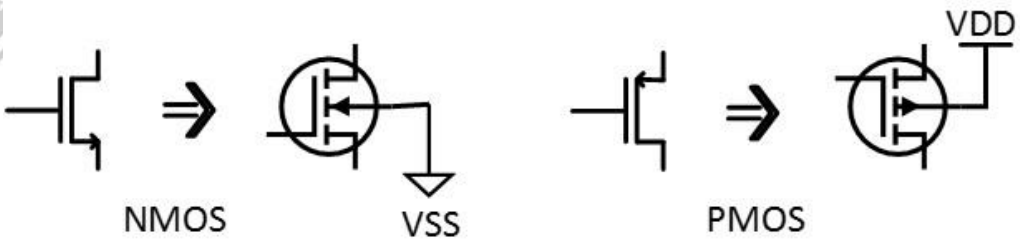

Figure 3. PMOS and NMOS back-gate connection

2.1.1 MOSFET's Physic

Figure 4 shows the diagram of MOS device physic. This MOS device is fabricated on a p-type substrate (as its body), and then n-regions is doped onto it. This will be forming a source and drain terminal. For the gate of this device, it is heavily doped of Poly-silicon and thin layer of Silicon Dioxide (SiO_2) in order to insulate the gate from the substrate [7].

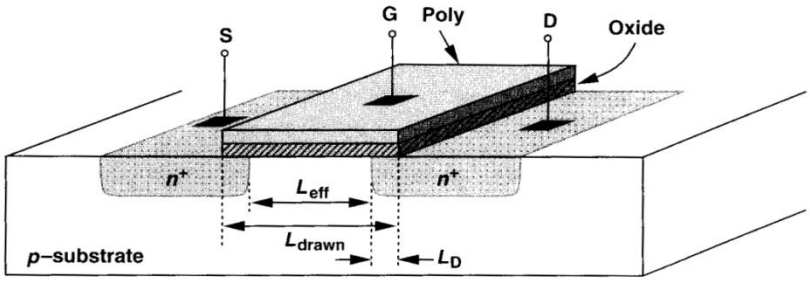

Figure 4. MOSFET's physic of *n*-type

For *width* of MOSFET, it is are the dimension of the gate along the source-drain path. *Length* of MOSFET is defined as the one which is perpendicular with width. Both of them are important parameter of MOSFET, known as W and L.

In spite of the fact that Figure 4 has a large scale of W and L, the actual size is in order nanometer. Furthermore, the improvement of nowadays technologies, making this size reduces until less of nanometer. However, the effective channel is slightly different from the drawn channel, especially in length case. This effective length channel is smaller due to fabrication's "side-diffuse". The amount of side-diffusion is noted as L_D and is shown in Equation 1.

$$L_{eff} = L_{drawn} - L_D \quad (1)$$

MOSFET's substrate is a greatly influence of the device characteristics. In typical MOSFET operation, the source and drain junction diodes have to be reverse-biased. NMOS substrate is connected to the most negative supply in the system so that PMOS will have reverse condition. The substrate connection is depicted in Figure 5.

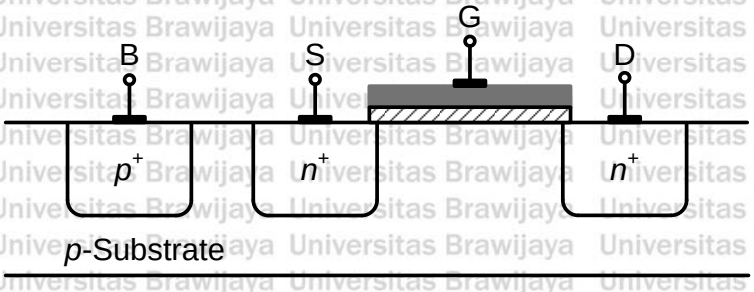

Figure 5. Substrate connection [12]

The action of device (such as current flow) takes a place in the substrate region under gate oxide. As shown in Figure 5, there are two structure of *n* doped region and both of them is symmetric. In order to distinguish drain and source, it needs to look on their carrier. Source is defined as terminal which is provided by charge carriers (electron for NMOS and hole for PMOS) whilst drain is the terminal that collect them. While voltages on terminals vary, drain and source may be changed.

In actual, PMOS and NMOS are packaged as one (and known as Complementary Metal Oxide Semiconductor or CMOS). They are fabricated on the same wafer. For this reason, one type is placed in a "well" and it is PMOS like what is shown in Figure 6.

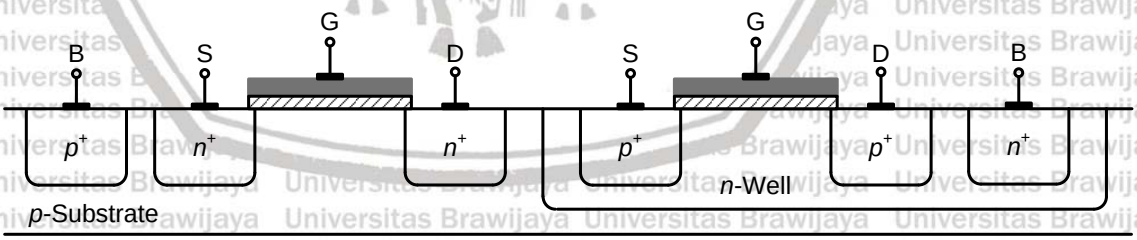

Figure 6. PMOS inside an *n*-well

2.1.2 MOSFET's Characteristic

There are various regions of MOSFET's operation depended on value of $V_{GS} - V_T$. For example, when $V_{GS} - V_T \leq 0$ or $V_{GS} - V_T$ has a negative

value, it means that MOSFET is in cutoff region and channels work as open circuit ($I_D = 0$). The other regions can be known based on Equation 2,

$$I_D = \frac{\mu_o C_{ox} W}{L}\left[(V_{GS} - V_T) - \left(\frac{V_{DS}}{2}\right)\right]V_{DS} \quad (2)$$

Where: μ is carrier effective mobility, C_{ox} is capacitance of the oxide layer per unit area, W is width of MOS transistor, L is length of MOS transistor, V_{gs} is gate-to-source voltage, and V_T is the threshold voltage of the MOS transistor.

Figure 7 shows the graphical illustration of MOS various $V_{GS} - V_T$'s result. This graphic is also known as graphic of modified *Sah*'s equation [13]. The top of each curve (maximal value) represents of the saturation value of MOS transistor. This point occurs while V_{DS} enters saturation. Not only that, this point acts as boundary of the other MOSFET's operation regions. This point equation is presented with Equation 3.

$$V_{DS\ (sat)} = V_{GS} - V_T \quad (3)$$

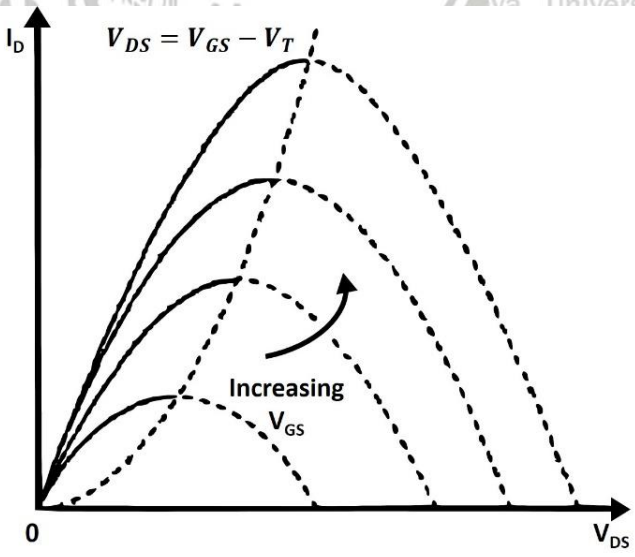

Figure 7. Graphical Illustration of MOS's V_{GS}-V_T various value

While V_{DS} has a value less than $V_{DS\,(sat)}$ but greater than V_{DS}=0, MOSFET works in triode/linear operation. In this region, current pass through from drain to source with its slope is proportional to $V_{GS} - V_T$. The curve bends because the channel resistance increase with V_{DS} and it gets saturated because the channel is pinched off at drain end, so that the amount of V_{DS} will not affected the increment of I_D anymore.

The area when V_{DS} is greater than $V_{DS\,(sat)}$ is called saturation region. In this kind of situation, while $K_n^{'} = \mu_o C_{ox}$, Equation 2 changes to

$$I_D = K_n^{'} \frac{W}{2L} \left(V_{GS} - V_T\right)^2 \quad (4)$$

Equation 4 elucidates if I_D will remain constant even though it is already passed through $V_{GS} - V_T$ state. However, in reality, it did not. At first, a little current is still present due to electromagnetic effect which is forcing electron to pass through against gradient potential. Furthermore, this current becomes bigger because of channel length's reduction while the V_{DS} value is increasing. This kind of phenomenon known as "channel length modulation". Thus, the I_D equation changes into:

$$I_D = K_n^{'} \frac{W}{2L} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right) \quad (5)$$

Which λ stands for typical coefficient channel length modulation (0.02 V^{-1}). This effect of channel length modulation is expressed in Figure 8.

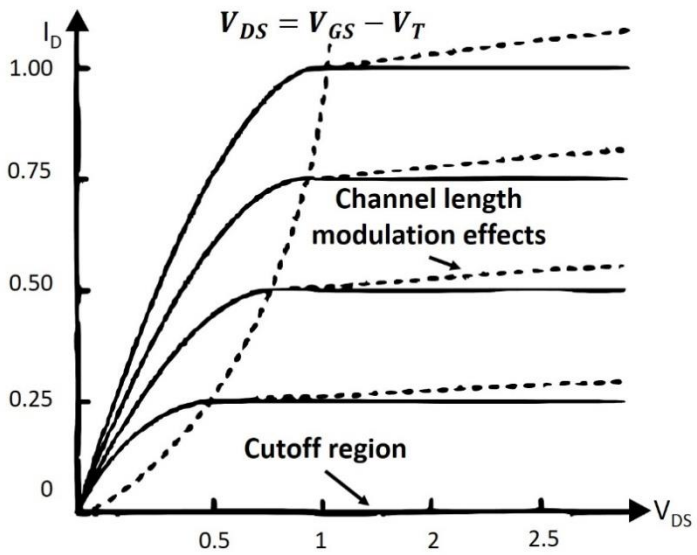

Figure 8. Channel length modulation effects in MOSFET characteristic

2.2 Noises

All of semiconductors devices have noises. They are known spread over in semiconductor itself. Noise itself has a definition as an unexpected fluctuation occurred in system. With respect to noise processes, it can be categorized as a random stochastic function in the function of time domain. Despite its randomness, average power and another properties of the noise manage to be observed through its "statistical model" even though its amplitude cannot. These spontaneous of fluctuations are unwanted parameter, it has to be reduced because they commit distortion onto the information.

As in for noise classification, it will be depended on the emphasis and the interest of the readers, the same materials are capable to be arranged in different ways [14]. Several of examples for noise classification are shown in [13-15]. Respectively, the classification of noise is chosen due to: its applicability in communication engineer that concerns in receiver noise [13], its components system quality [15], and the places where the noise generates [16].

2.2.1 MOSFET's Noises

Several type of noises present on MOSFET, the most important source for noise are thermal noise, shot noise, generation-recombinant noise, *1/f* noise, $1/f^2$ noise, burst or random telegraph signal (RTS) noise and avalanche noise [17]. However based on phenomenology, they are four main types as MOSFET's fundamental noise: thermal noise, shot noise, generation-recombinant noise and low frequency noise or is often called as *1/f* noise.

For modeling noise, usually noiseless component or even system is used and connected into current or voltage source or even both of them. These sources are intended for noise sources representation.

Equivalent diagram of MOSFET with attached noise source is shown in Figure 9 and Figure *10*. They stand for MOSFET with current noise source modeling and input noise voltage modeling, respectively. These figures consist of thermal and *1/f* noise. There, noises are replaced with one source which is their summation result. The only differences is in what form they are represented.

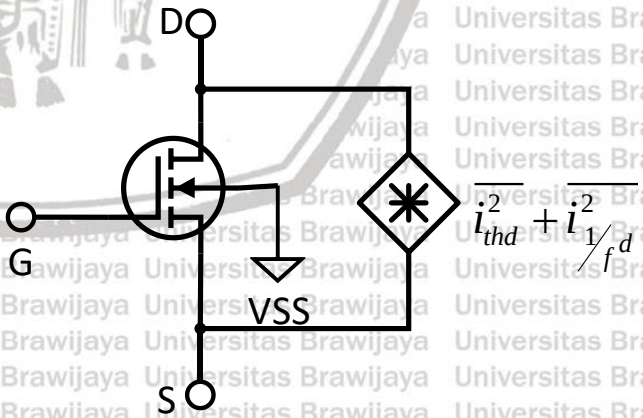

Figure 9. Current noise source modeling

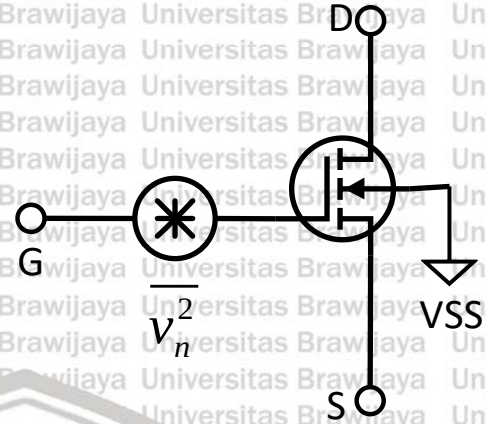

Figure 10. Input noise voltage modeling

Thermal and *1/f* noise have their own representation. Equation 6 and 7 stands for intensities of current source replacement for thermal noise and *1/f* noise, respectively.

$$\overline{i_{thd}^2} = 4kT\left(\frac{2g_m}{3}\right)\Delta f \tag{6}$$

$$\overline{i_{1/f\,d}^2} = \frac{Kg_m{}^2}{WLC_{ox}f}\Delta f \tag{7}$$

As for equivalent current noise source, it is the summation of Equation 6 and 7. It is expressed into Equation 8, while input noise voltage can be formed like Equation 9, where K is a *1/f* noise constant of process dependent on the order of 10^{-25} V^2F on the bandwidth of 1 Hz and k = $1.38x10^{-23}$ J/K as the Boltzmann constant.

$$\overline{i_n^2} = \overline{i_{thd}^2} + \overline{i_{1/f\,d}^2} = \left(\frac{8}{3}kTg_m + \frac{Kg_m}{WLC_{ox}}\frac{1}{f}\right)\Delta f \tag{8}$$

$$\overline{v_n^2} = \frac{\overline{i_{thd}^2} + \overline{i_{1/f\,d}^2}}{g_m^2} = \left(\frac{8}{3g_m}kT + \frac{K}{WLC_{ox}}\frac{1}{f}\right)\Delta f \quad (9)$$

Using some knowledge of how the MOSFET fabricated so it can trigger some noises, which will be explained in next section, the equivalent small signal analysis can be drawn for MOSFET transistor (shown in Figure 11)[18].

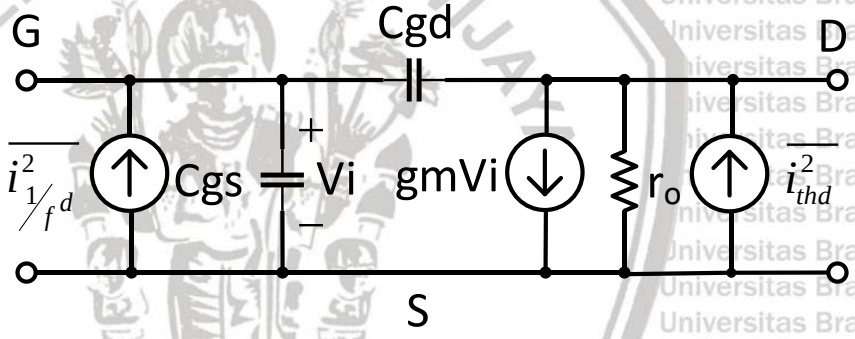

Figure 11. MOSFET's small signal noise

In reality, Operational Amplifier (Op-Amp) system contains a lot of MOSFET inside. The modeling of its noise is shown in Figure 12 while the modeling of outside noise such as thermal noise from resistor is added, will be expressed in Figure 13[19]. The magnitude of them are typically on $nV/\sqrt{Hz}$ or $pA/\sqrt{Hz}$.

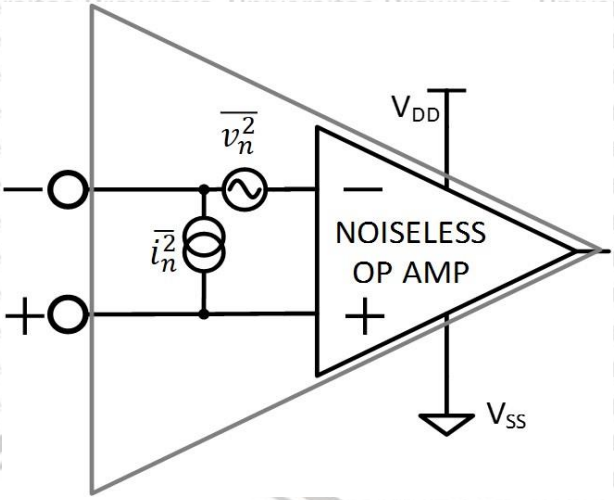

Figure 12. Noiseless Operational Amplifier system

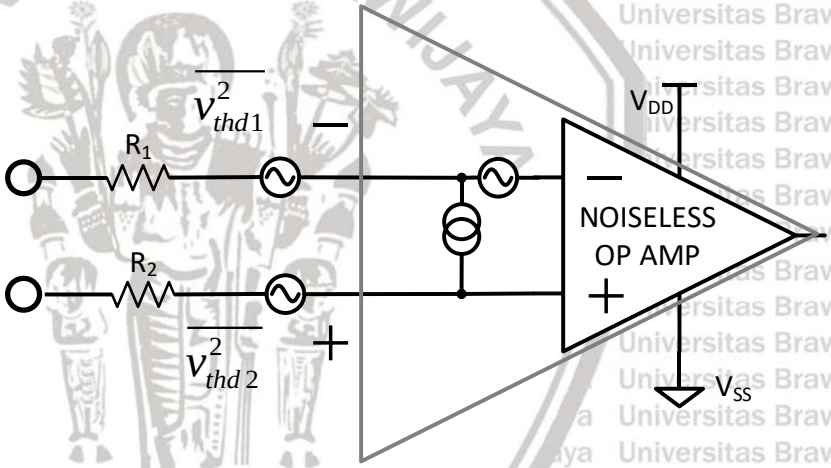

Figure 13. Modeling of noise while output operational amplifier noise is taken into account

2.2.2 *1/f* Noise

Flicker noise or also known as pink noise or *1/f* noise is dominating low frequencies. Even though the frequency ranges are very low and up to 10^{-6} Hz, flicker noise still can be found. It disturbs all semiconductor devices. MOSFET and CMOS is one kind to suffer a lot. The intensities of *1/f* noise is larger than thermal noise for frequency below 1-10 kHz [20]. In application, the amount of *1/f* noise is not only larger than thermal noise, it

is still bigger than all present noises combined together (white noise). The intersection of white noise and *1/f* noise is called f_{knee}. In this point, *1/f* noise and white noise are equal to each other. Figure 14 is shown of noise spectrum. It is explained if the power spectral density (PSD) function of *1/f* noise is proportional to frequency in inverse state (like what Equation 7 states) or can be expressed as:

$$S(f) = \frac{1}{f^{\alpha}} \tag{10}$$

Where the value of α is vary in range 0.7-1.3 typically.

The vertical axis (y-axis) of Figure 14 as a function frequency f, represents the intensity of current sources or input noise voltages ($\overline{i_n^2}/\Delta f$, $\overline{v_n^2}/\Delta f$). If $f < f_{knee}$, then *1/f* noise is the dominant noise component, and if $f > f_{knee}$ the white noise is the prevailing noise on the device. The expression of f_{knee} due to respect to thermal noise can be written as,

$$4kT\left(\frac{2g_m}{3}\right)\Delta f = \frac{Kg_m{}^2}{WLC_{ox}}\frac{1}{f_{knee}}\Delta f \tag{11}$$

That is,

$$f_{knee} = \frac{K}{WLC_{ox}} g_m \frac{3}{8kT} \tag{12}$$

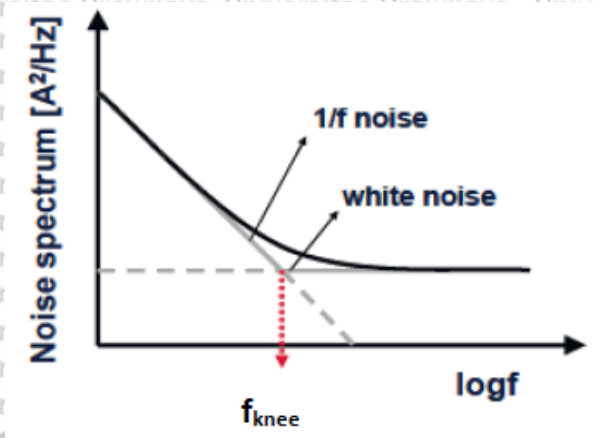

Figure 14. Spectrum of noises.

1/f noise is associated with material failures or its imperfections during fabrication. Depending how *1/f* noise occurs in devices, there are two ways to model it: *Surface Model* and *Bulk Model* developed by McWhorter in 1957 [21] and Hooge in 1969 [22], respectively.

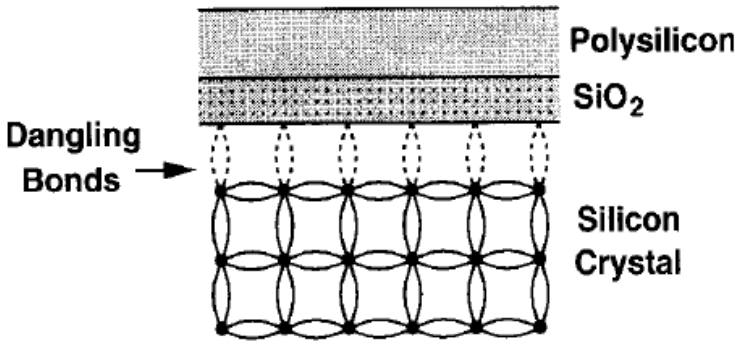

Figure 15. Si/SiO_2 interface

In case of MOSFET and CMOS, the *Surface Model* suits them better than the other. *1/f* noise on these devices has directly connected into interface of Silicon Crystal (Si) and Silicon Oxide (SiO_2) quality. Since Si is ended at this interface, many "dangling bonds" (shown in Figure 15) appears and randomly trapped some charge when it pass through there. This charge will be released in time that cannot be predicted. This kind of condition triggers flickering energy occurs in the drain current.

The amount of *1/f* noise increases along with the reduction of device size. That is why, quality and reliability of devices usually seen from the resistances of the device itself to *1/f* noise or how much it level corrupted in the device. From the equations and *1/f* noise spectrum, can be concluded if *1/f* noise gets reduced, the other noise which is included in white noise will be also reduced.

PMOS is the well-known of MOSFET transistor which exhibit less *1/f* noise than NMOS transistor. The reason is, PMOS transistor carry holes in a "buried-channel".

2.3 Operational Amplifier

2.3.1 Differential Amplifier

Differential amplifier (DA) has a lot of advantageous over single-end operation. First, DA has higher immunity to noise. Second, DA increases maximum achievable voltage swing. Third, DA also has simpler biasing and higher linearity, and many others.

DA is built from two schematics refer to the way it gives output signal, from two point or one point. Two point is differential output DA and one point is single-ended DA. They are shown in Figure 16 (a) and (b), respectively. In case of differential output, the value of output is subtraction of both side output (plus and minus). In case of single-ended output, it is the simplification of differential output. M3 and M4 in Figure 16 (a) act as current sources. They have same value, which can be replaced by using current mirror. This technique will give single-ended output which is expressed in Figure 16 (b).

In order to calculate gain of both of schematics, small signal is used. Figure 17 and Figure 18 are the small signal for DA differential output and DA single-ended output. Using nodal analysis, and substituting each node, the amplification will be expressed exactly in Equation 16 and 20.

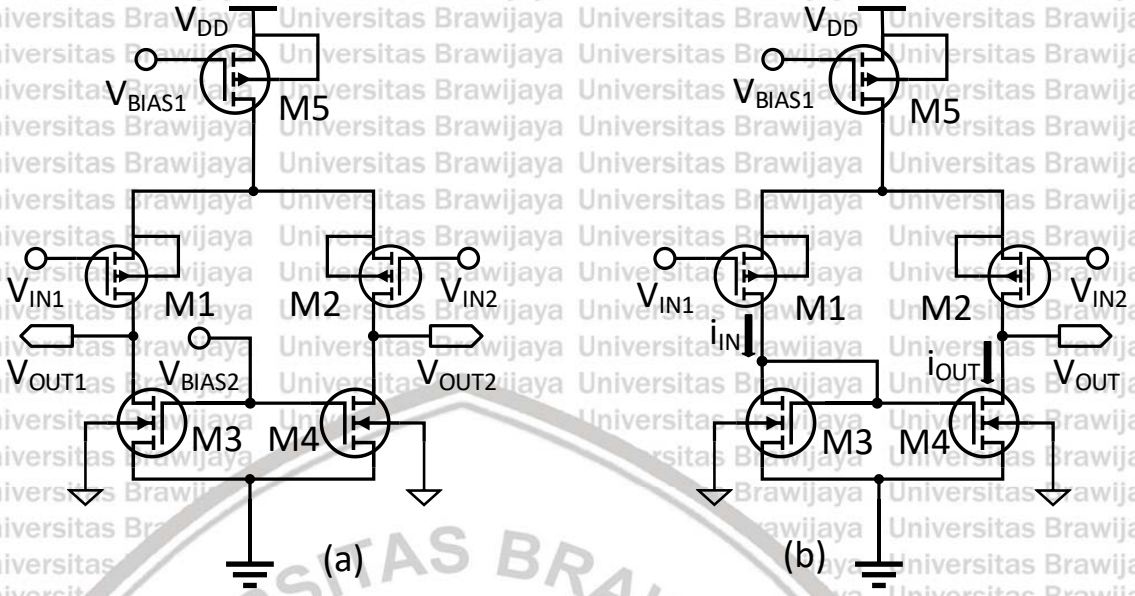

Figure 16 (a) Schematics of differential amplifier differential output and (b) single-ended output

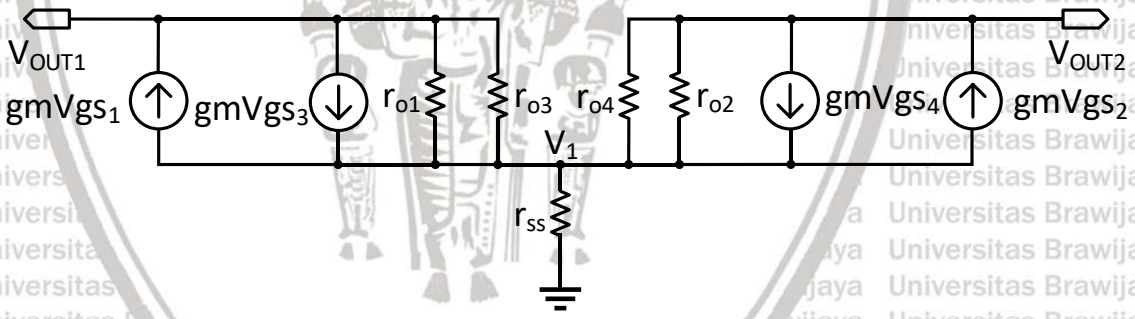

Figure 17. Small signal analysis of DA differential output

Node analysis at node V_{OUT1}

$$\frac{1}{r_{o1} \parallel r_{o3}}(V_{OUT1} - V_1) - gm(V_{IN1} - 2V_1) = 0 \quad (13)$$

Node analysis at node V_{OUT2}

$$\frac{1}{r_{o2} \parallel r_{o4}}(V_{OUT2} - V_1) - gm(V_{IN2} - 2V_1) = 0 \quad (14)$$

Node analysis at node V_1

$$\frac{V_1}{r_{SS}}+\frac{V_1-V_{IN2}}{r_{o2}\parallel r_{o4}}+gm(V_{IN2}-2V_1)+\frac{V_1-V_{IN1}}{r_{o1}\parallel r_{o3}}+gm(V_{IN1}-2V_1)=0 \quad (15)$$

Due to the value of M3=M4 and M1=M2 and the dominant power in circuit system, the gain of DA differential output is expressed by

$$\frac{V_{OUT1}-V_{OUT2}}{V_{IN1}-V_{IN2}}=gm\left(r_{o2}\parallel r_{o4}\right) \quad (16)$$

As for single ended output, $V_{GS3}=V_{GS4}$, $V_{G3}=V_{D3}$. This condition is called current mirror. Current pass through M1will have a same value with current into M4 ($i_{IN}=i_{OUT}$). Therefore the small signal of M3 is equivalent with $\frac{1}{gm}\parallel r_{o3}$. Due to M1 and M3 serial condition, the small signal of single-ended output is

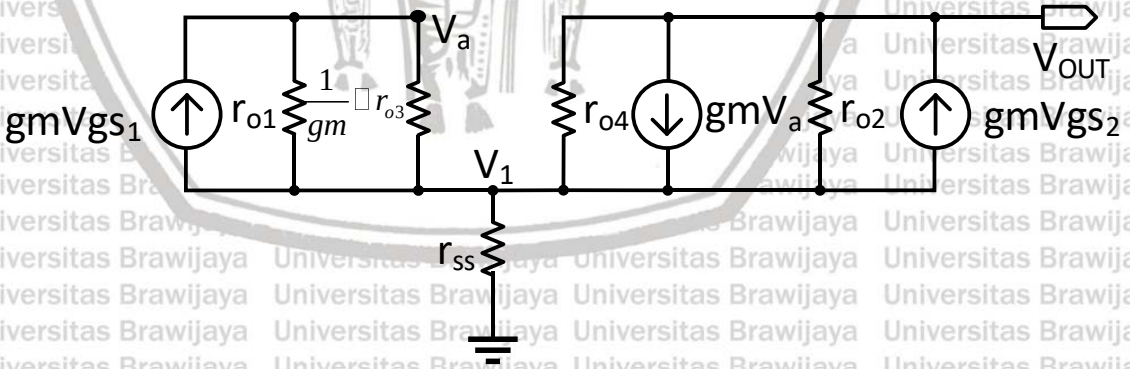

Figure 18. Small signal analysis of DA single-ended output

Small signal analysis for Figure 18 is evaluated using node analysis. According to this analysis, equation for node at Va:

$$\frac{1}{r_{o1} \parallel \left(\frac{1}{gm} \parallel r_{o3}\right)}(V_a - V_1) - gm(V_{IN1} - V_1) = 0 \quad (17)$$

Node analysis at node V_{OUT}

$$\frac{1}{r_{o2} \parallel r_{o4}}(V_{OUT} - V_1) - gm(V_{IN2} - V_1) + gmV_a = 0 \quad (18)$$

Node analysis at node V_1

$$\frac{V_1}{r_{SS}} + \frac{V_1 - V_{IN2}}{r_{o2} \parallel r_{o4}} + gm(V_{IN2} - V_1) - gmV_a + \frac{V_1 - V_a}{r_{o1} \parallel \left(\frac{1}{gm} \parallel r_{o3}\right)} + gm(V_{IN1} - V_1) = 0 \quad (19)$$

Due to the value of M3=M4 and M1=M2 and the dominant power in circuit system, the gain of DA single-ended output is expressed by

$$\frac{V_{OUT}}{V_{IN1} - V_{IN2}} = \left(-gm\left(r_{o1} \parallel \frac{1}{gm}\right)\right)\left(gm\left(r_{o2} \parallel r_{o4}\right)\right) = gm\left(r_{o2} \parallel r_{o4}\right) \quad (20)$$

2.3.2 Two Stage Operational Amplifier

DA has a high gain, however its swing is limited because of the transconductance of DA inputs and the high output impedance. The second stage is added to make a wider swing [7]. According DA's schematics above, two stage of operational amplifier can be drawn as Figure 19 and Figure *20*. They have differential output and single-ended output, respectively.

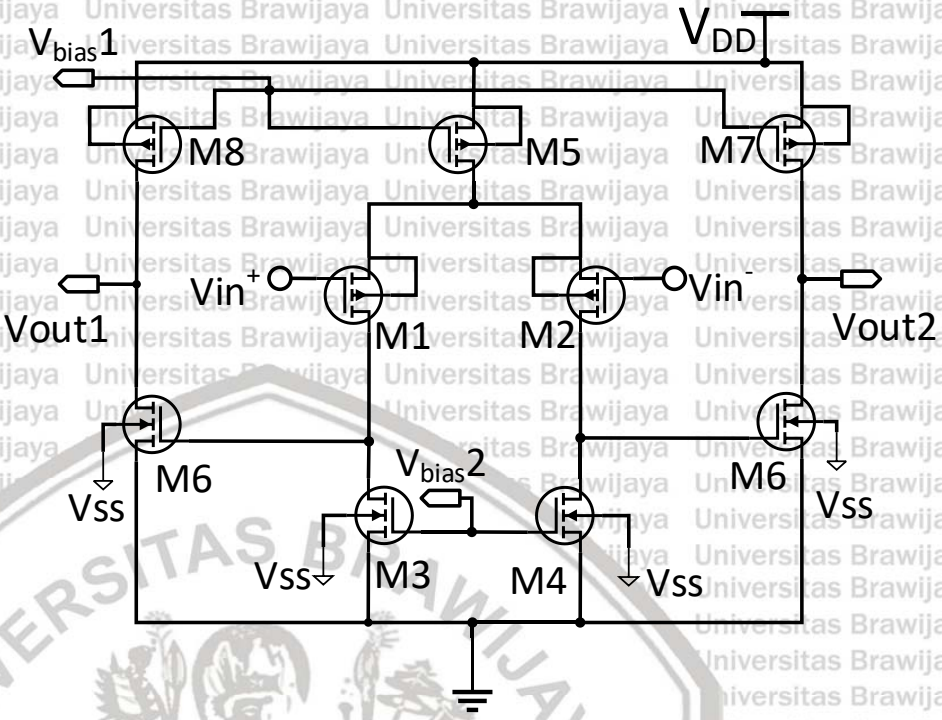

Figure 19. Differential output two stage operational amplifier

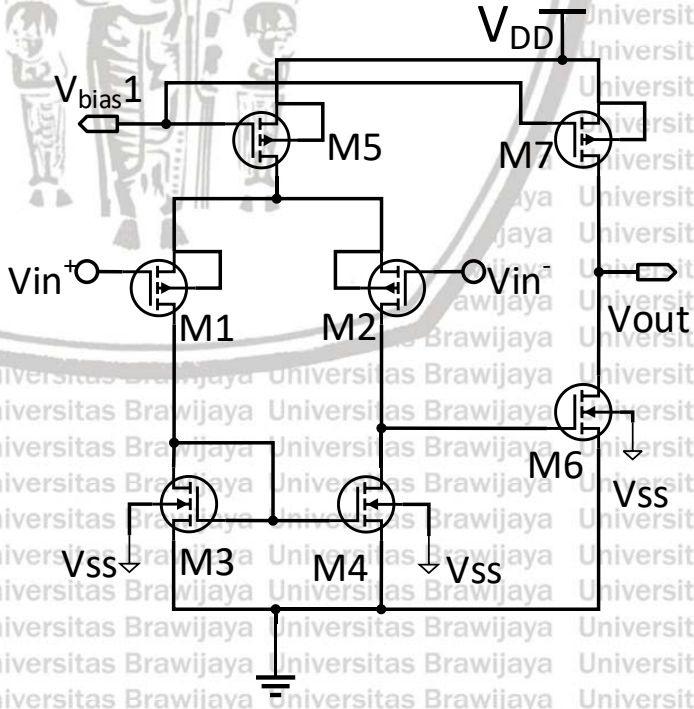

Figure 20. Single-ended output two stage operational amplifier

Both of these two stage operational amplifier's schematics are widely used. Application of the schematics are depended on the placement and the purposes. However, single-ended two stage operational amplifier is commonly used in technologies in order to simplify and shrink device size.

Therefore, it is well known that Two Stage Operational Amplifier has 2 poles. These poles (GO_{p1} and GO_{p2}) appear because of the capacitance parasitic. These poles affect operational amplifier perform greatly [23]. Using diagram bode, its responses can be drawn. Every pole cost -20 dB/decade in gain margin and 45° in phase shift. Figure 21 shows small signal if the parasitic capacitance is include and Figure 22 shows the bode-plot of it [13].

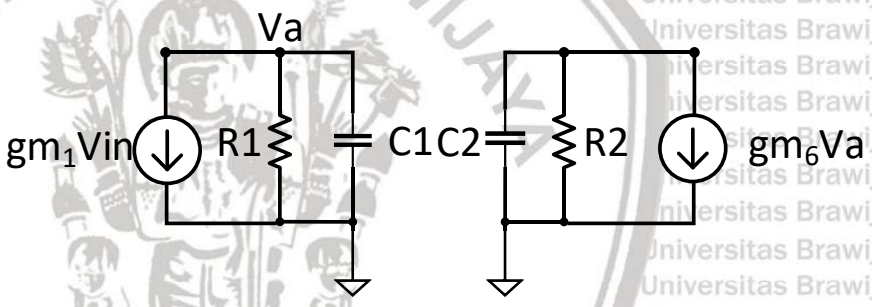

Figure 21. Small signal of Two Stage Operational Amplifier

Where:

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$
$$C_2 = C_{db6} + C_{db7} + C_{gd7}$$
$$R_1 = ro_2 \square ro_4$$
$$R_2 = ro_6 \square ro_7$$
$$R_1, R_2 << gm_6$$

Using nodal analysis, gain of this operational amplifier can be derived.

$$\frac{Vout}{Vin} = \frac{gm_1 gm_6 R_1 R_2}{\left(1 - \frac{s}{\frac{1}{C_1 R_1}}\right)\left(1 - \frac{s}{\frac{1}{C_2 R_2}}\right)} \quad (21)$$

$$which - \frac{1}{C_1 R_1} is\ \omega_{p1}, - \frac{1}{C_2 R_2} is\ \omega_{p2}$$

Figure 22 below states that GB (unity gain) has very small gap (phase margin) with Y-axis 0°. It means that this circuit does not stable. The smaller phase margin will make larger overshot occurred in system. However, in the same time, bigger phase margin can cost time in circuit processing. Phase compensation is needed to overcome this problem. Basically, phase margin ranges at least on 45°, preferably 60° or larger.

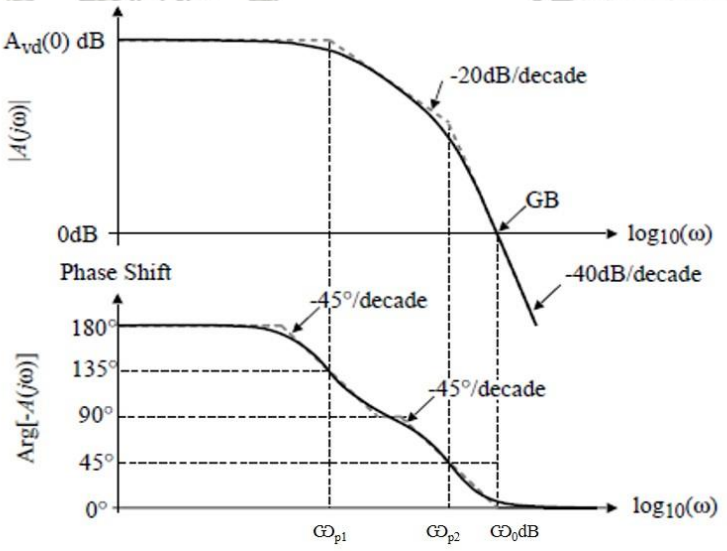

Figure 22.Bode-plot of single-ended output without phase compensation

In order to stabilize two stage operational amplifier, phase compensation is applied. It will split poles and make phase margin higher.

Basically, phase margin ranges at least on 45°, preferably on 60° or larger. While phase compensation is added like what is shown in Figure 23 below, the equivalent small signal is presented in Figure 24.

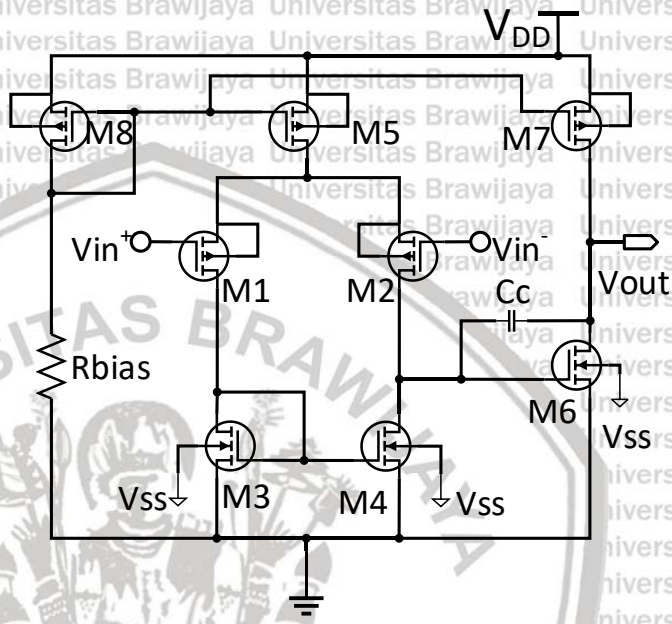

Figure 23. Two stage operational amplifier compensated

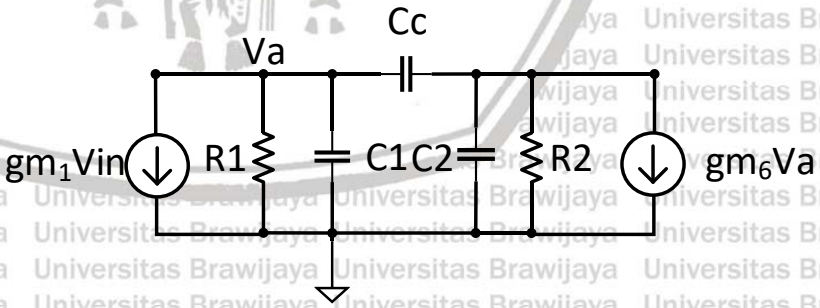

Figure 24. Small signal operation amplifier compensated

Using nodal equation, the gain can be found. Inside of the gain exist the representation of poles.

$$\frac{Vout}{Vin} = \frac{gm_1 gm_6 R_1 R_2 \left(1 - \frac{s}{\frac{gm_6}{C_c}}\right)}{\left(1 - \frac{s}{-\frac{1}{gm_6 C_c R_1 R_2}}\right)\left(1 - \frac{s}{-\frac{gm_6}{C_2}}\right)} \quad (22)$$

$$\omega_{p1} = -\frac{1}{gm_6 C_c R_1 R_2}$$

$$\omega_{p2} = -\frac{gm_6}{C_2}$$

$$\omega_z = \frac{gm_6}{C_c}$$

$$A_{DC} = gm_1 gm_6 R_1 R_2$$

ω_{p1} and ω_{p2} have new values. This is the indicated that poles were already splitting. This conditions changes both phase margin and gain margin. Then the bode-plot become Figure 25.

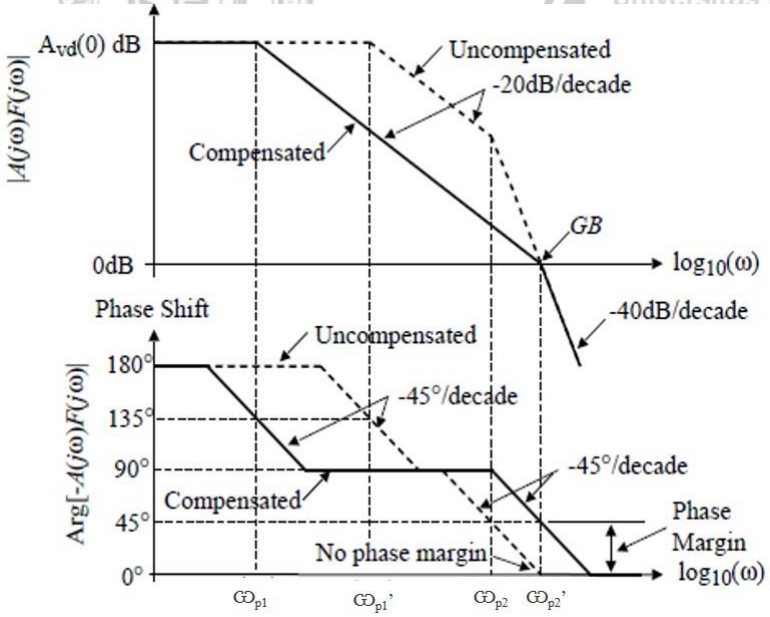

Figure 25. Bode-plot of single-ended output compensated

2.4 Chopper Stabilization Technique

Mentioned before, *1/f* noise is one kind of crucial noise to operational amplifier performance. This noise has to be reduced. Chopper Stabilization Technique or know as CST is one of method to eliminate noise. It is schematically built from switches and has two inputs (in respect to a pair input signal) then two outputs.

Basically, CST works in continuous time with 2 CSTs. 1st CST will modulate signal input to high frequency with AC modulation signal. Then 2nd CST demodulates input signal while modulates *1/f* noise to high frequency band after both of them got amplified. After that, filter cut *1/f* noise to eliminate its effects [24]. This work's scheme of CST is shown in Figure 26 with *m(t)* is modulation controller, blue arrow is the representation of input signal, *Vn* and pink triangular stands for *1/f* noise and green line is defined for low pass filter.

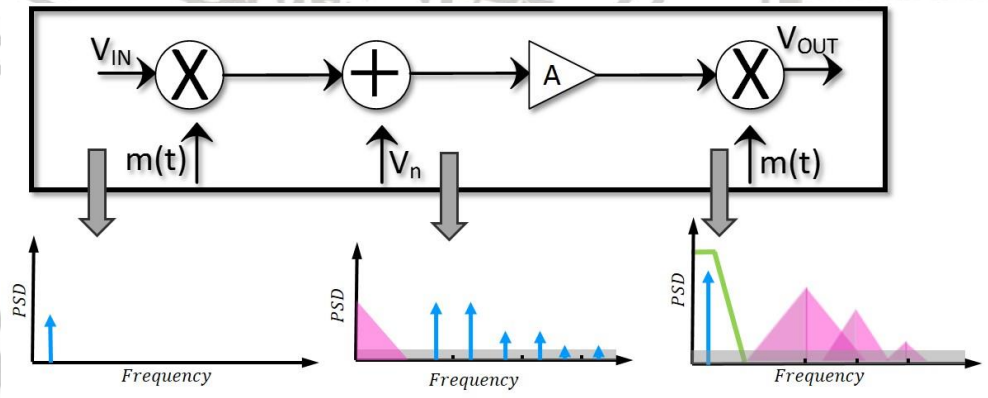

Figure 26. CST scheme of works

CHAPTER III
PROPOSED CIRCUIT

3.1 Problem

Instrumentation Amplifier (IA) consist of three Differential Amplifier (DA) and 7 resistors in general. According to common knowledge, IA has a high Common Mode Rejection Ration (CMRR), high input impedance and configurable differential gain. However, IA has some drawbacks such as sensitive CMRR in respect of resistor mismatches, offset voltage and *1/f* noise disturb and limit its performance and bandwidth will narrow itself when high closed-loop gain is applied [3].

As mentioned in chapter 2, noises in operational amplifier cannot be avoided. Thermal noise, *1/f* noise, offset voltage and the others have to be reduced in order to get better performance. CST is one of the techniques to reduce them. In order to overcome noise problems, at first CST is tried to be employed into IA. Figure 27 shows its schematics. However, the problems of IA which is mentioned before, still remains. Fully Balance Differential Difference Amplifier-Differential Difference Amplifier (FBDDA-DDA) is proposed to improve IA performance. In FBDDA-DDA schematics, CST is also implemented to cancel offset voltage and *1/f* noise. Its schematic is shown in Figure 28.

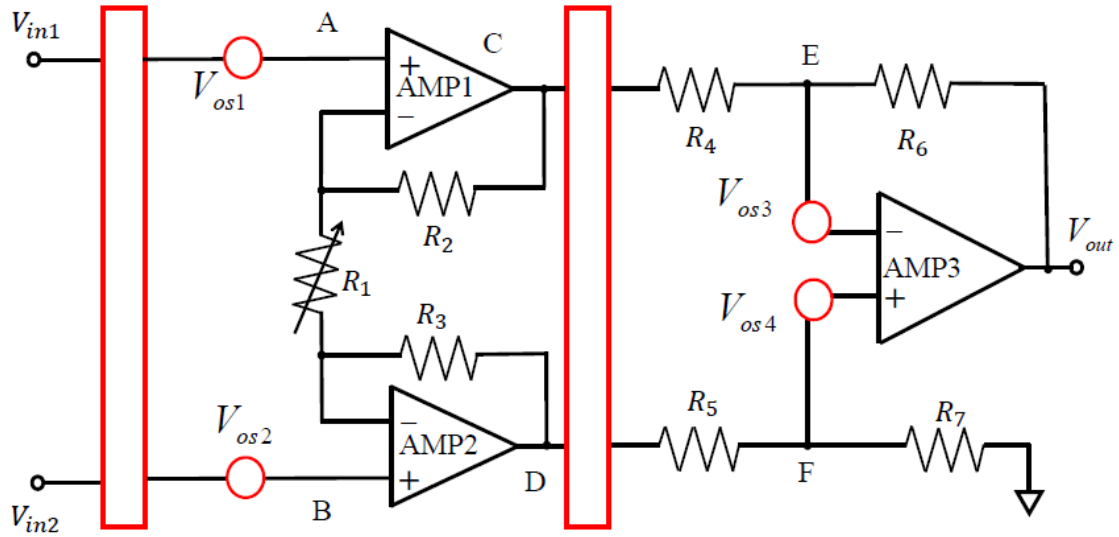

Figure 27. IA schematic with CST implementation

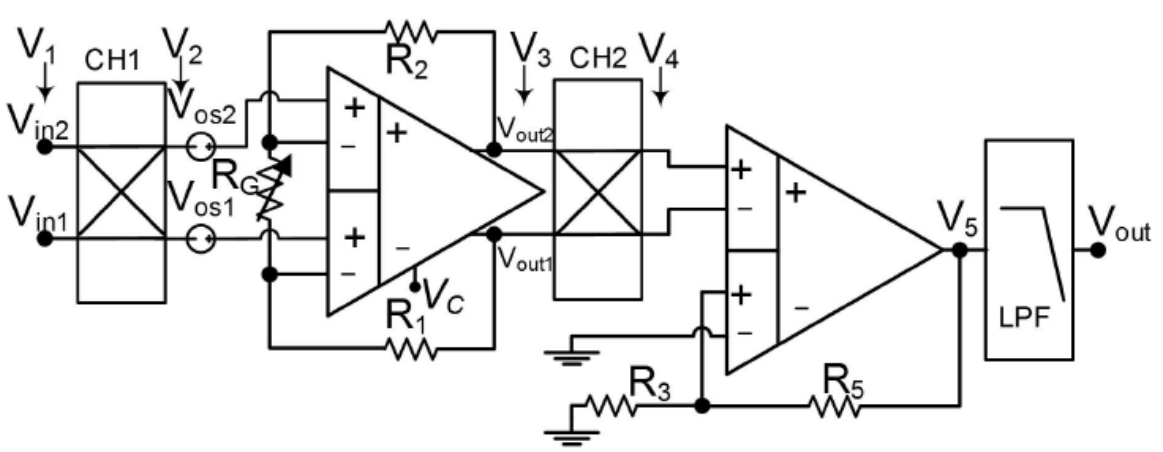

Figure 28. FBDDA-DDA schematic with CST implementation

Like its name, FBDDA-DDA was built from two blocks: FBDDA and DDA which for each blocks are shown in Figure 29: (a) as FBDDA and (b) as DDA. From Figure 29, it is noted that FBDDA and DDA consists of 4 terminal inputs. However, FBDDA has differential output while DDA has single-ended output. FBDDA and DDA combination are shown in Figure 30.

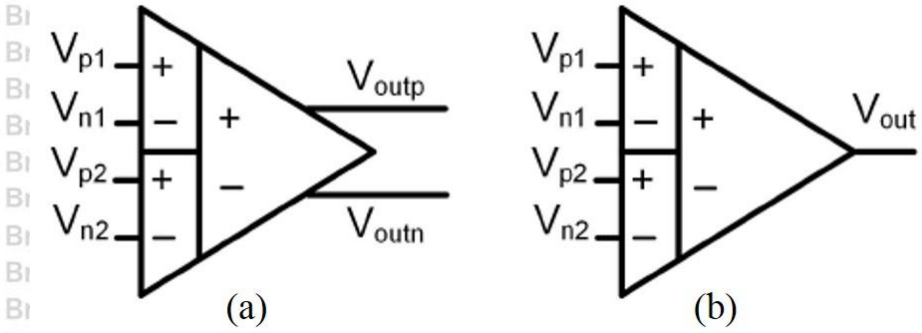

Figure 29 (a) FBDDA symbol (b) DDA symbol

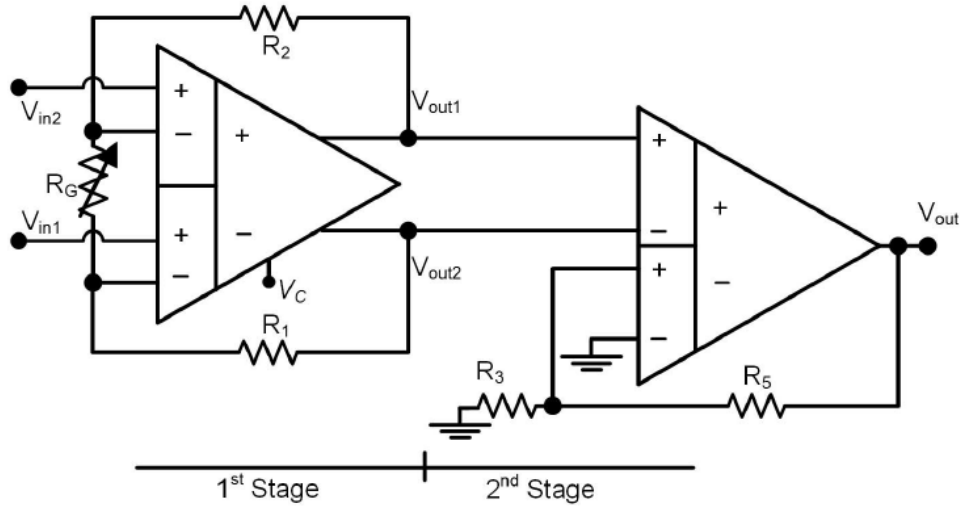

Figure 30. Combination of FBDDA and DDA without CST influences

However, even though FBDDA-DDA is built in order to replace IA, CST placement only for FBDDA. Same case is happened in IA, CST is placed in input-output of AMP1 and AMP2. According to common knowledge, the disturbances in AMP1-AMP2 or FBDDA is the most important to be reduced. However, practically amplifiers have inside noises. MOSFETs are built inside of them, and MOSFET contains a lot of noises. This noises certainly are needed to be reduced.

3.2 Proposed System

As mentioned before, even though using FBDDA-DDA, noises (including *1/f* noise) on the last amplifier (DA for IA and DDA for FBDDA-DDA) will not be reduced. However, *1/f* noise is one kind of serious problem because of its characteristics such as dominating low frequencies and cannot predicted.

CST explained in Chapter 2 is one of the most effective solution to overcome the problem. A general CST can be applied to differential input and differential output circuits, however, the output of DDA is single ended. Therefore, CST cannot be applied directly. In this chapter, new CST to apply to differential input and single-ended output circuit based on the folded cascode operational amplifier is proposed.

3.2.1 Folded Cascode Operational Amplifier

Linearity is one of most important parameter for operational amplifier because it can affect its precision. One of technology for increasing linearity in operational amplifier is by adding feedback on its system. However, one of the drawback this technology is oscillation will occur due to its parasitic capacitance and mirror pole in DA presences.

Equation 16 and 20 reverse to the amplification of DA without taking into account the modulation of channel length and its effect into DA's current flows. It is important to be noted that the inputs of DA (respect to Figure 16) is supposed to be $V_{GS1}=V_{GS2}=V_{DS1}$. However, V_{GS2} may have different value so that those I_{IN} and I_{OUT} in Figure 16 will not have same value. Cascoding DA like Figure 31 (a), will overcome this problem. Further, it will increase the gain of DA.

Figure 31 (a) is a folded cascode operational amplifier. Indeed, using telescopic cascode gives more benefits to system. However, it is not suitable for small frequency, moreover it has tail current which limit its swing, an additional pole, and it has to be stacked so V_{OUT} and V_{IN} cannot be shorting. Two stage of folded cascode (cascoding amplifier and current mirror) are applied in order to achieve higher gain even though it will cost its swing.

In order to determine the output of folded cascode amplifier (Voltage of point h of Figure 31) the method like prior DA (in chapter 2) is used. In this case, because Figure 31 has symmetrical structure, Z_{OUT} is presented into Equation 23. Figure 32 shows its small signal equivalent circuit so that nodal analysis can be applied there.

$$Z_{OUT} = \left[gm_6 ro_6 \left(ro_4 \| ro_2 \right) \right] \| \left[gm_8 ro_8 ro_{10} \right] \quad (23)$$

thus, the amplification of this circuit is shown in Equation 24,

$$\frac{V_{OUT}}{V_{IN}} = gm_1 \left[gm_6 ro_6 \left(ro_4 \| ro_2 \right) \right] \| \left[gm_8 ro_8 ro_{10} \right] \quad (24)$$

In order to transmit the signal input to output perfectly and to make the swing larger, output of folded cascode (V_{OUTh}) is connected into class AB common source. Class AB common source schematic is shown in Figure 31 (b).

The benefits using class AB common source are high current drive ability during slewing and hence it has large slew rate [25]. Also, Class AB common source can be categorized as second stage of operational amplifier, while folded cascode is the first stage of operational amplifier.

As shown in Figure 31 (b) M1' and M2' work as a level shifter, then M3' and M4' work as class AB common source push-pull amplifier. The amplification of class AB common source amplifier can be calculated using its small signal and nodal analysis, refers to Figure 33.

With $V_a = -\frac{gm_{1'} V_{IN}}{\frac{1}{ro_{1'} \| ro_{2'}}}$, the amplification is,

$$\frac{V_{OUT}}{V_{IN}} = \left(gm_{3'} + gm_{4'} \right) \left(ro_{3'} \| ro_{4'} \right) \quad (25)$$

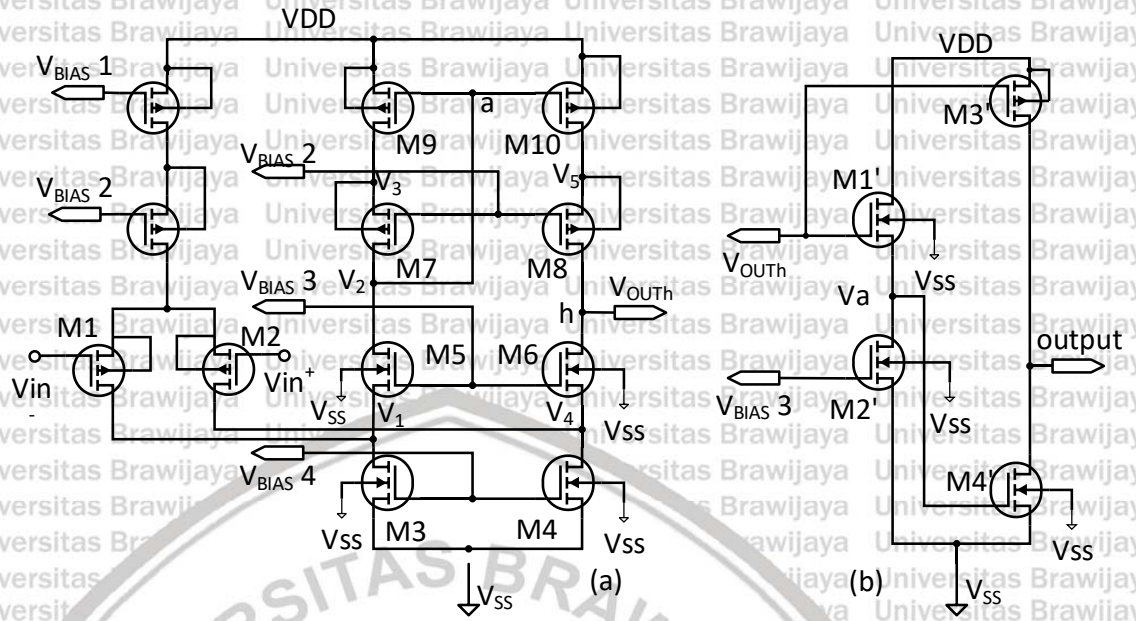

Figure 31. (a) Folded cascode operational amplifier (b) class AB common source

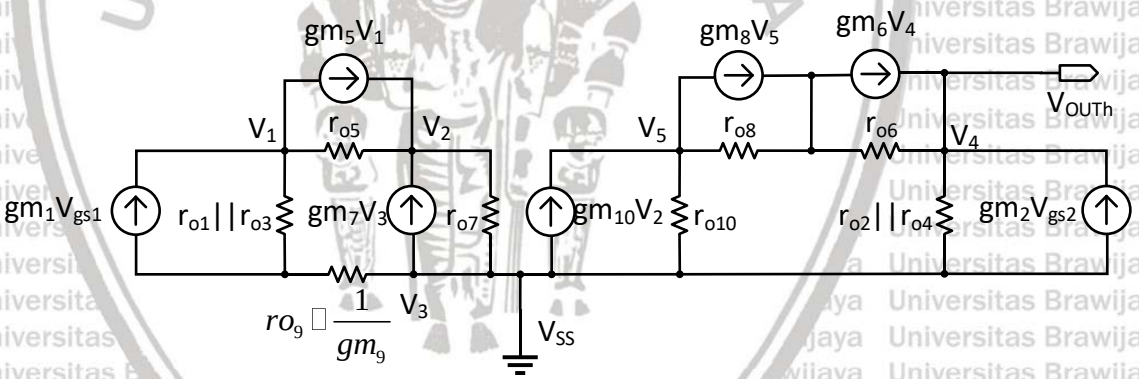

Figure 32. Small signal folded cascode operational amplifier

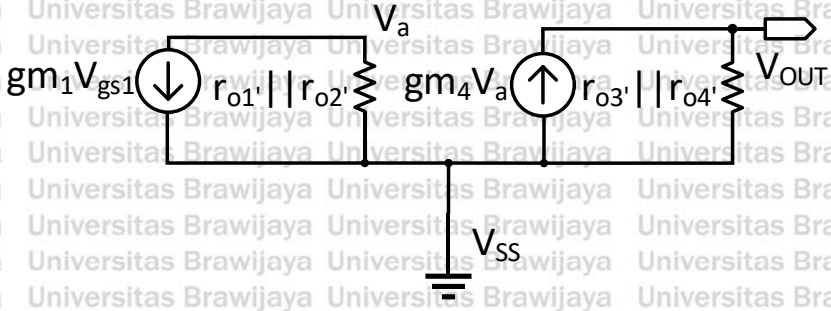

Figure 33. Small signal of class AB common source

Figure 34 shows the connection between circuit folded cascode amplifier (as 1st stage of operational amplifier) and class AB common source (as 2nd stage of operational amplifier). Figure 35 shows the complete circuit of folded cascode amplifier, class AB common source and bias circuit whereas this bias circuit is calculated so the stability of it does not affected with another addition component. Phase compensation is added to the circuit in order to maintain the stability while the feedback is applied (after operational amplifier output) and to split the poles that is occurred in V_2, h and output of class AB common source amplifier points. On Figure 35, Rc and Cc are the representation of phase compensation with value 2k and 14 pF, respectively. The amplification under the low frequency band is,

$$\frac{V_{OUT}}{V_{IN}} = gm_1\left(gm_{3'} + gm_{4'}\right)\left(ro_{3'} \,||\, ro_{4'}\right) \left[gm_6 ro_6 \left(ro_4 \,||\, ro_2\right)\right] \,||\, \left[gm_8 ro_8 ro_{10}\right] \quad (26)$$

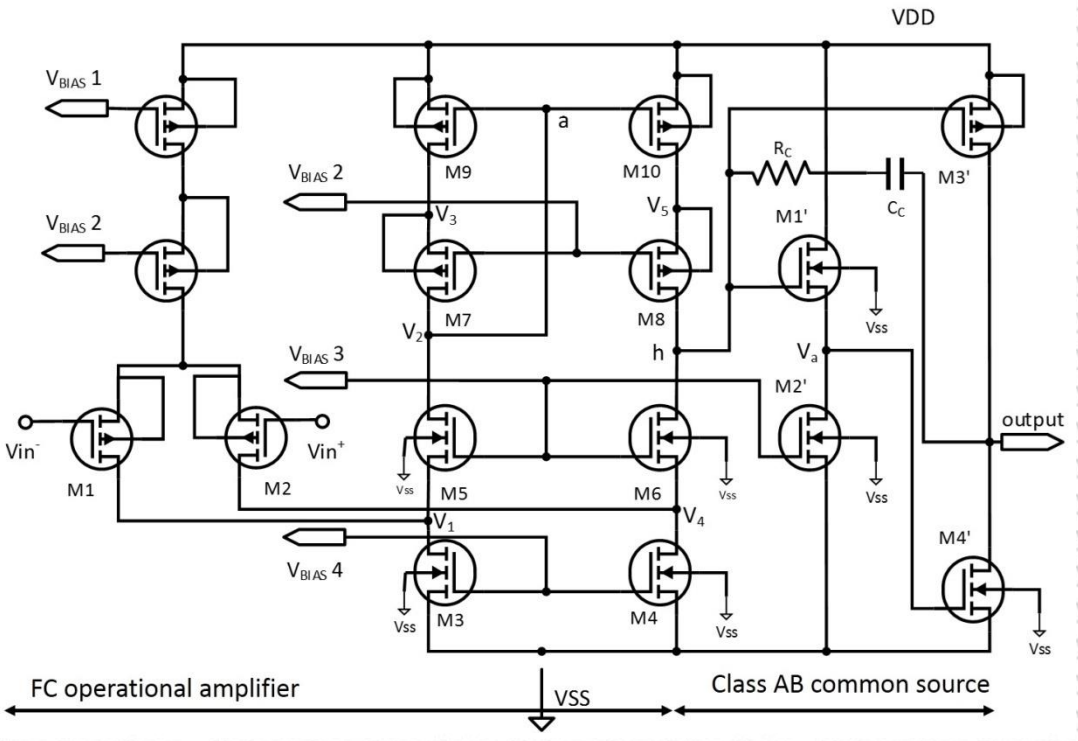

Figure 34. Combination of folded cascode operational amplifier with class AB common mode amplifier

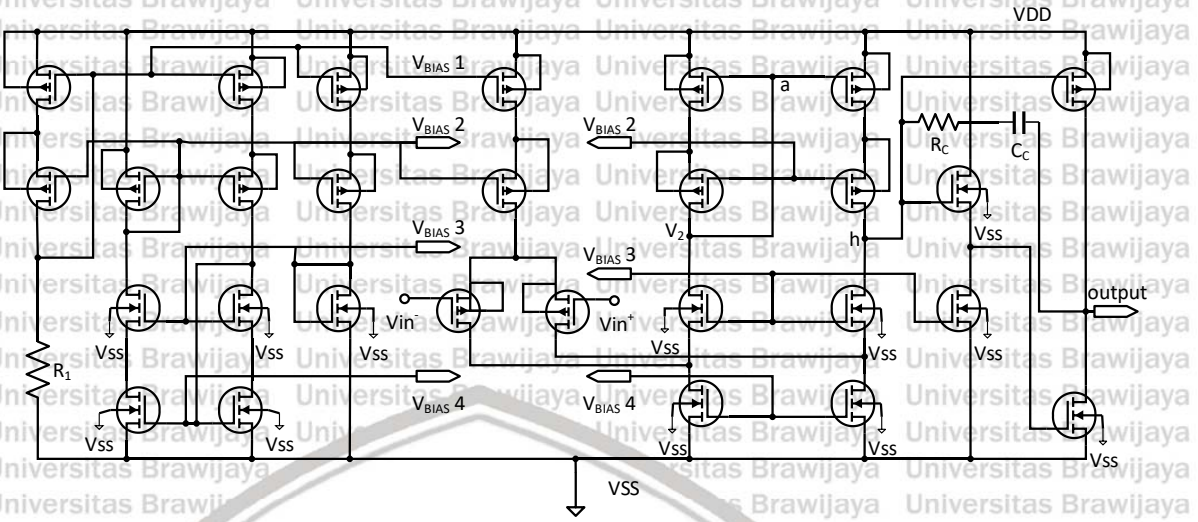

Figure 35. New operational amplifier scheme

3.2.2 Application of Chopper Stabilization Technique to Folded Cascode Operational Amplifier

Mentioned in chapter 2, usually CST has two inputs and two outputs. This condition is used to place CST on conventional IA or FBDDA-DDA technique (refers to Figure 27).

Theoretical analysis can be explained from Figure 36 which is respect to each point of *a*, *b*, *c*, and *Vout*. It starts with signal inputs ($V_{in^+} = V_{in} \sin \omega_{in} t$ and $V_{in^-} = -V_{in} \sin \omega_{in} t$) enter the chopper 1. Each chopper is built from switches using CMOS technologies (is shown in Figure 37). Then clock signals operate the switches and input signals are modulated into high frequency. Condition ON and OFF on Figure 36 stand for different phase of clock signals *CLK* and $\overline{CLK}$. Using Fourier series *g*(t) and –*g*(t), *CLK* and $\overline{CLK}$ can be expanded. Where *g*(t) is written in Equation 27 and contains chopping frequency inside. Then the modulation signal of point *a* is represented into Equation 28.

Vn as *1/f* noise representation is found before modulated signal inputs enter amplifier. Basically point *b* is the signal after noise been applied. After that two signals outputted from amplifier at point *c*, they have been amplified. The condition of this signals are shown in Equation 29. Then each signal

pass through second CST. This chopper works as modulator for *1/f* noise and demodulator for input signals. Equation 30 is shown its process. As for output system, Vout is described in Equation 31. The *Vn* can be removed by using Low Pass Filter (LPF).

$$g(t) = \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{2n-1}(2n-1)\omega_c t \tag{27}$$

$$V_{a_{1,2}} = \pm 2V_{in}\sin\omega_{in} tg(t) \tag{28}$$

$$V_{b_1} = V_{a_1} = 2V_{in}\sin\omega_{in} tg(t) \tag{29}$$
$$V_{b_2} = -2V_{in}\sin\omega_{in} tg(t) + V_n$$

$$V_{c_1} = 2AV_{in}\sin\omega_{in} tg(t) \tag{30}$$
$$V_{c_2} = -2AV_{in}\sin\omega_{in} tg(t) + V_n$$

$$V_{OUT_1} = A\left(V_{in}\sin\omega_{in} t\right) \tag{31}$$
$$V_{OUT_2} = A\left(V_{in}\sin\omega_{in} t + 2V_n g(t)\right)$$

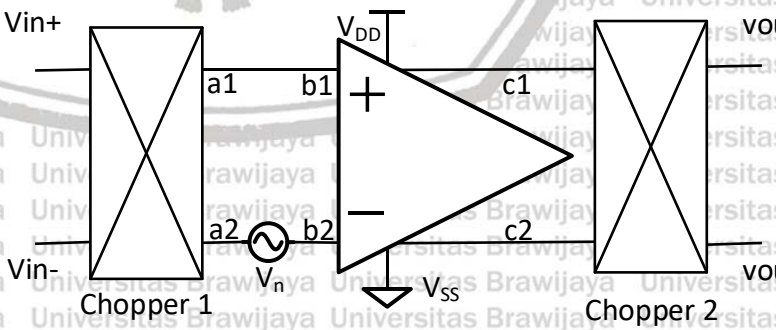

Figure 36. Implementation of CST to operational amplifier

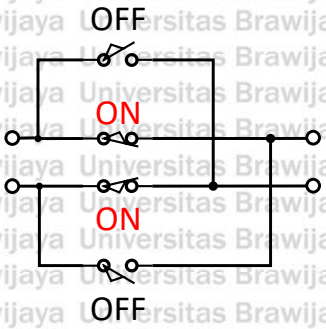

Figure 37. General chopper stabilization technique schematic

Regularly, CST has differential output like the explanation before. This condition is the reason why CST cannot be implemented into DA (in conventional IA) or DDA with single-ended output. However, both of DA and DDA need CST for reducing *1/f* noise inside themselves. In order to overcome this problem, new CST showed in Figure 38 is proposed to replace the general CST of Figure 36. Details of switches inside this CSTs are expressed in Figure 39. Using this kind of switches placement, CST can be implemented into single-ended output of amplifier such as DA or DDA.

Proposed CST's process is not different with general CST. The slightly differences only in where demodulated signal inputs and modulated *1/f* noise (second CST) processes happen. In case of new CST, second CST placement is in output of first stage amplifier (folded cascode). And then V_{OUTh} works as differential output. Class AB common source that is placed as second stage of operational amplifier has a role to maintain output by push-pulling output from the folded cascode amplifier, so that the current flows perfectly. The influences of *Vn* in the output can be removed using LPF.

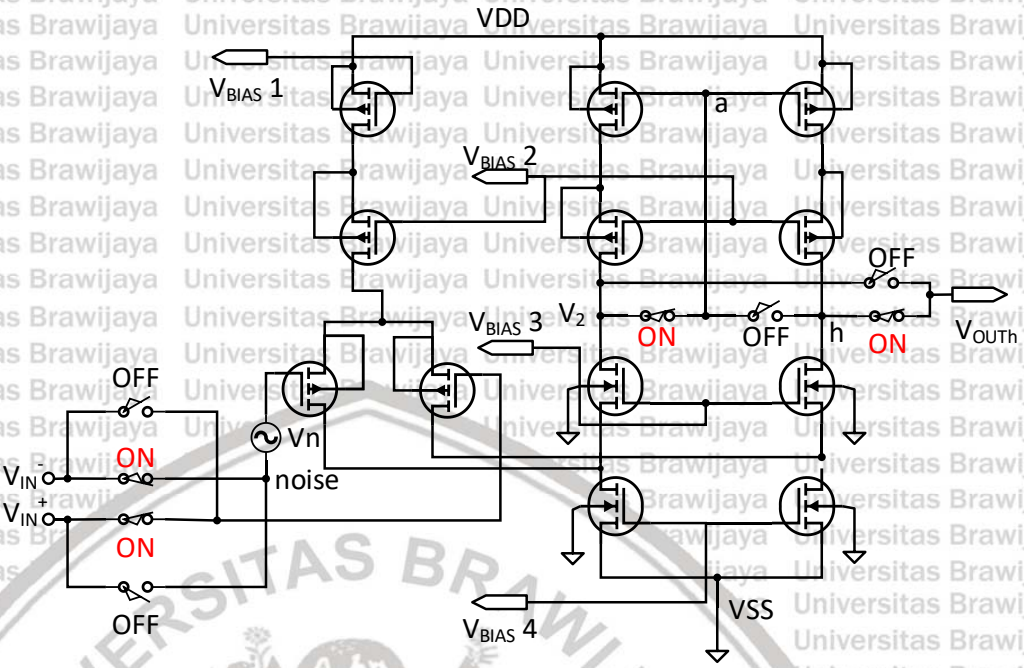

Figure 38. Proposed schematic of CST

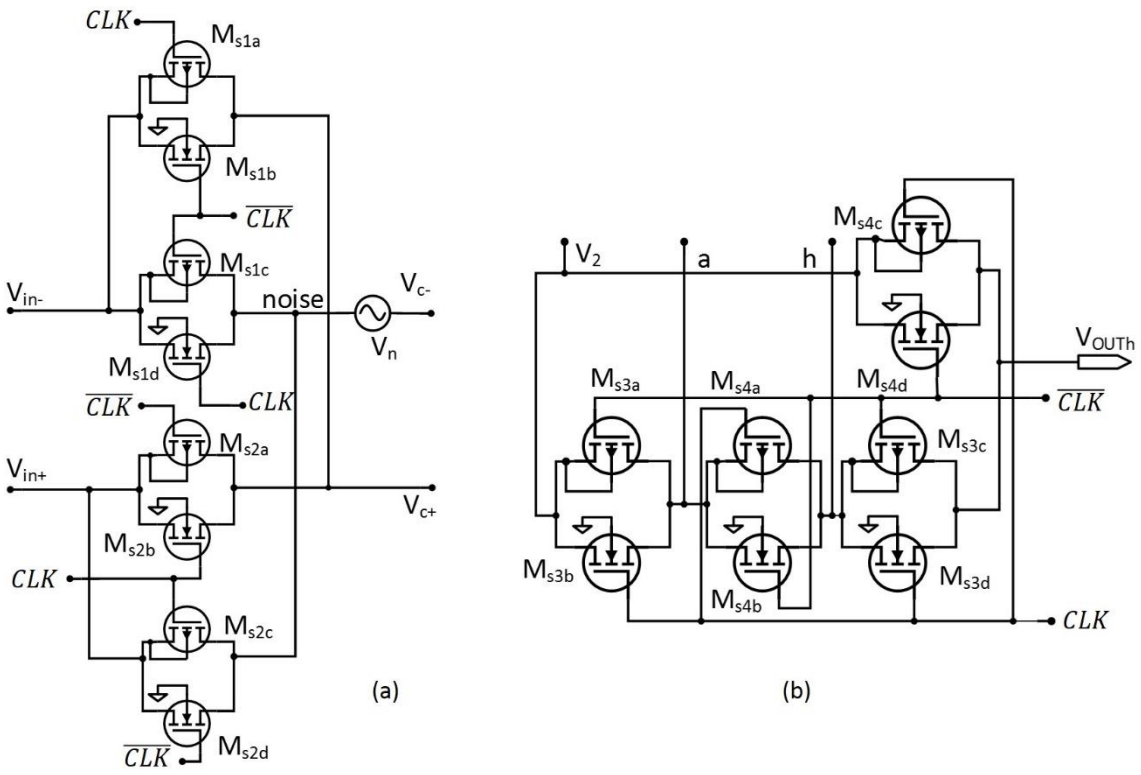

Figure 39. The placement of switches inside CSTs: (a) chopper 1 (b) chopper 2

3.2.3 Operational Amplifier Cell

In prior sub chapter, it is already explained about combination of folded cascode amplifier, class AB common source as second stage operational amplifier and CST. Using three of them, separation of *1/f* high gain, stable responses, wide bandwidth and large swing can be achieved.

In order to remove *1/f* noise, Low Pass Filter (LPF) has to be added into system and placed after feedback point. Analogue Standard 6th order Gm-C OTA LPF is used because the perfect sinusoidal signal is wanted. The signal frequency is chosen based on a condition of $f_{input} < f_{filter} < f_{chopping}$. It is detailed in Equation 32.

$$f_{filter} = \frac{1}{2\pi RC} = \frac{gm}{2\pi C} \tag{32}$$

Final schematic of combined all proposed system including LPF is expressed into Figure 40. This system will be packed as one. It is named "Low *1/f* Noise Operational Amplifier Cell" and is shown in Figure 41.

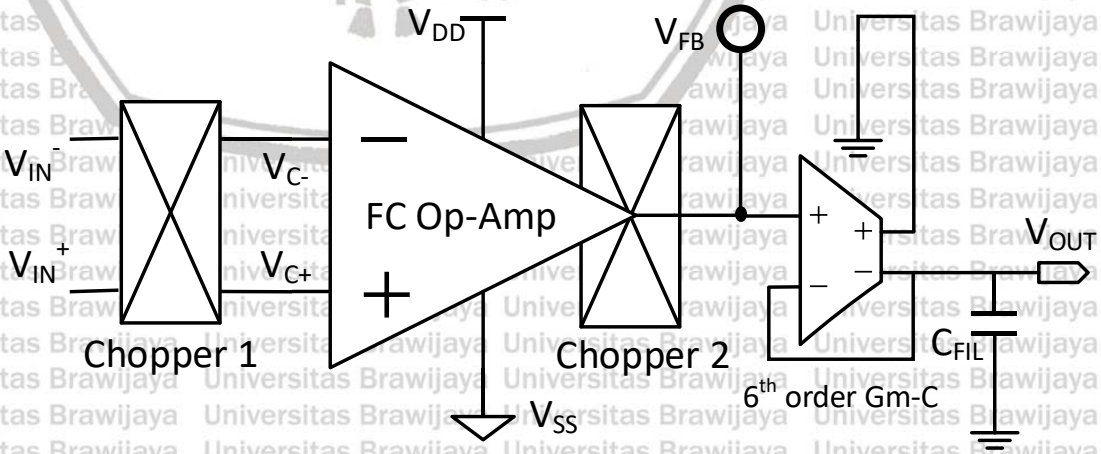

Figure 40. Schematic low *1/f* noise operational amplifier cell

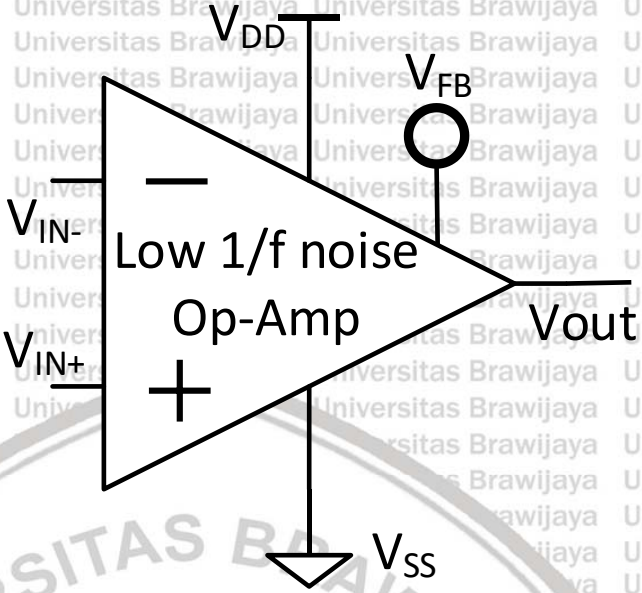

Figure 41. Low *1/f* noise operational amplifier cell

CHAPTER IV
ANALYSIS AND RESULTS

The circuit proposed in this master thesis was designed by using a 0.6 µm CMOS process and evaluated by using HSPICE. The basic condition of simulation is listed in Table 1. Furthermore the parameters for each MOSFETs transistor inside of proposed operational amplifier cell was set like Table 2.

Table 1. Simulation conditions

Item	Value
V_{DD}	2.5 V
V_{SS}	-2.5 V
Frequency of V_{IN}	100 Hz
Frequency of CLKs	10 kHz
Frequency of 6^{th} *order LPF*	1 kHz
Frequency Vn	20 Hz, 40 Hz, 60 Hz
Amplitude of Vn*'s 20 Hz*	10 mV
Amplitude of Vn*'s 40 Hz*	1 mV
Amplitude of Vn*'s 60 Hz*	0.1 mV
Amplitude of V_{TEST}	±5 mV
R_1	92.5 kΩ
R_C	2 kΩ
C_C	14 pF

Table 2. Parameters of proposed operational amplifier cell

Item	Value
W/L NMOS [µm]	1.6/2.6
W/L PMOS [µm]	5.2/2.6
W/L Input [µm]	47.8/2.6

This master thesis simulation is evaluated in transient and Fast Fourier Transform (FFT) analysis. However, HSPICE does not have *1/f* noise features in transient or FFT analysis. Therefore, in order to achieve *1/f* noise performance, some signals has to be added to represent *1/f* noise. Based on Figure 14, these additional signals set on 20 Hz, 40 Hz, 60

Hz and their amplitude are 10 mV, 1 mV and 0.1 mV. Thus, *1/f* noise representation under FFT analysis of these additional signals is shown in Figure 42.

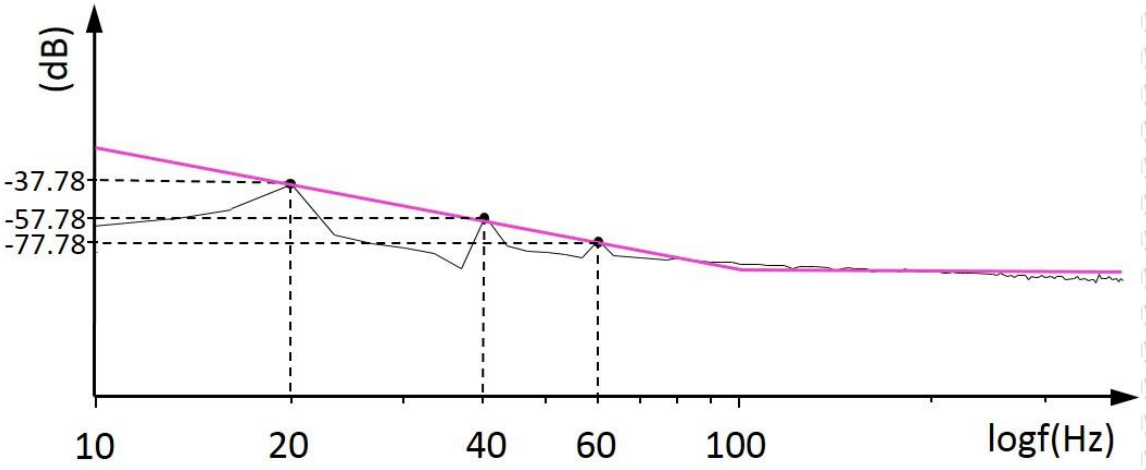

Figure 42. *1/f* noise representation

4.1 Folded Cascode-Chopper Stabilization Technique

The purpose of this simulation is to make sure that the performance of the proposed system is still within the range of expectation, especially after the operational amplifier is added by the new CST system. Figure 43 (a) and (b) are evaluation circuit diagram for AC analysis. The results from this simulation can be seen in Figure 44 and Figure 45. This figures explain that performance of the proposed system is still within the expectation.

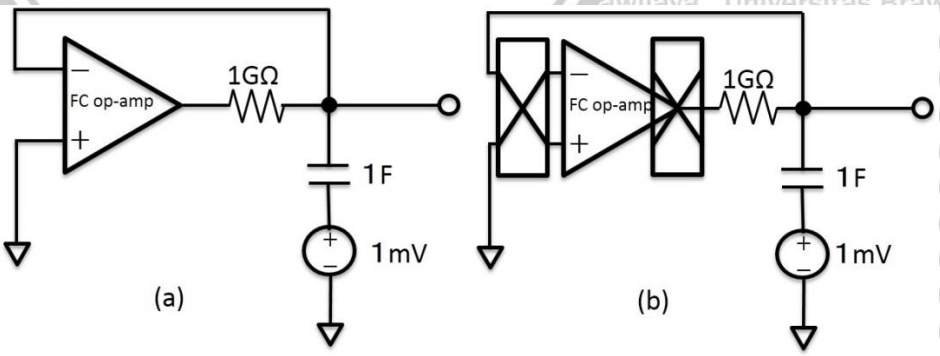

Figure 43. Circuit simulation of Op-Amp operation (a) and combination of Op-Amp and new CST (b).

In Figure 44, the different performance of operational amplifier system and the one combined with new CST system (proposed circuit) when both of them is simulated in 0 dB and in -3 dB for determining bandwidth, can be seen. A few differences in the form of phase margin also can be found. The detailed results from this simulation can be summarized in the Table 3. As for Figure 45, the gain of 1 Hz (DC gain) on both of them is shown.

Table 3. Comparison op-amp and op-am-new CST

Item	Op-Amp	Op-Amp—new CST
Bandwidth	3.939 Hz	1.675 Hz
Phase Margin	60.785°	58.018°
Gain	128.43 dB	126.56 dB
Frequency of unity gain	12.238 MHz	3.023 MHz

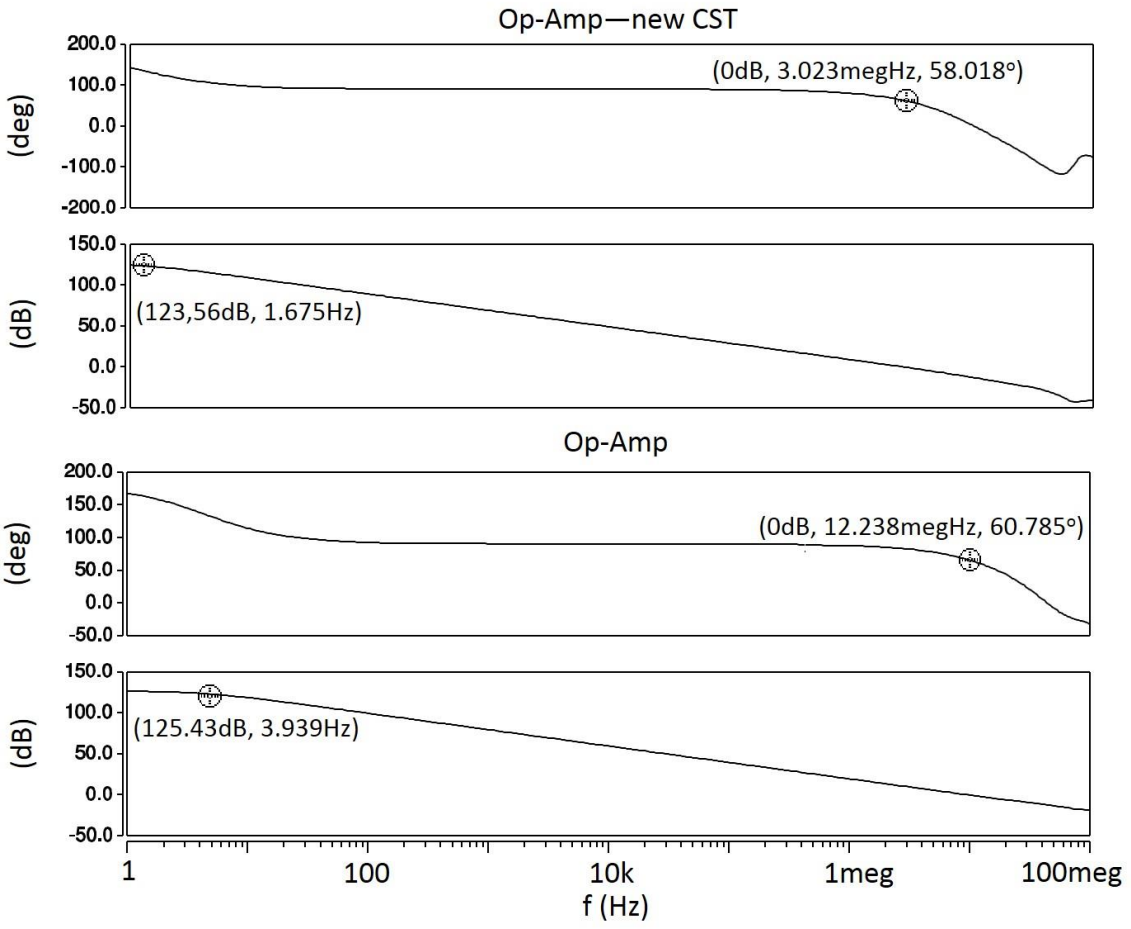

Figure 44. Bandwidth and phase margin comparison

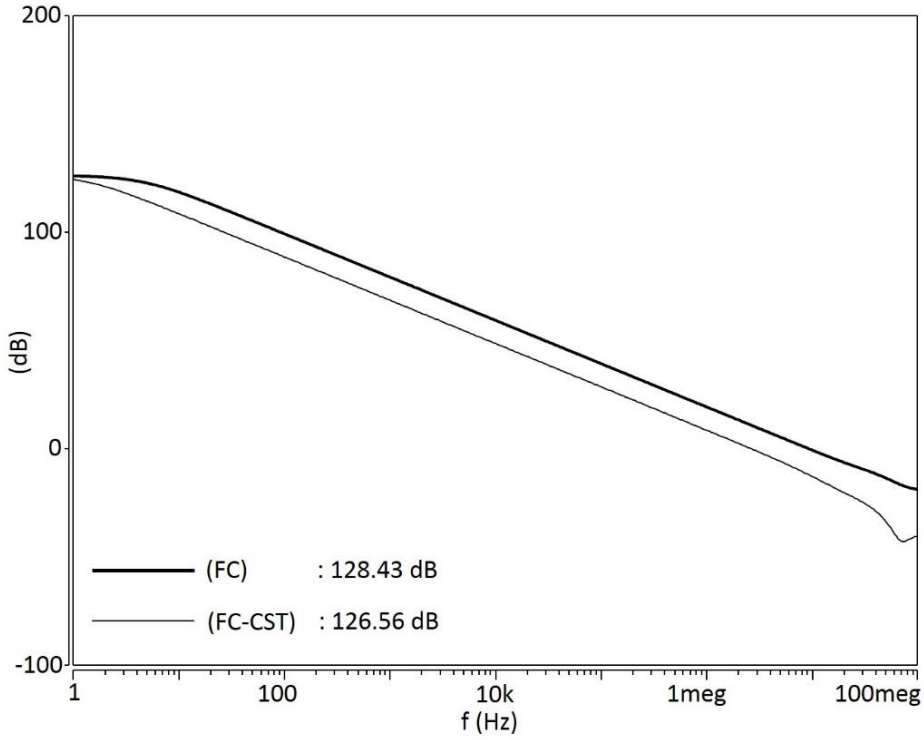

Figure 45. Gain comparison

From results of Table 3, adding new CST system on the operational amplifier will change the bandwidth, phase margin and the gain. However, these changes will not effect the overall performance of the proposed system. The reasons are: First, this proposed circuit even though has a narrow bandwidth, it will not affect system operation because in reality, bandwidth is determined by the amount of negative feedback. Second, due to this narrow bandwidth, operational amplifier has high gain. Losing 2.87 dB of gain is still better than worsen the stability. Because in order to have a higher gain, it will cost in phase margin. Third, losing 2.767^{o} in phase margin will not affect too much in stability. According to Chapter 2, in order to have stable response, phase margin is needed to have at least more than 45^{o}.

4.2 Practical Implementation

Using implementation of proposed circuit in actual amplification circuit was one way to analyze the signal in each point and the quality of this proposed circuit. The simplest of amplification circuit is inverting amplifier, which is shown in Figure 46. Theoretical amplification of inverting amplifier is,

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_f}{R_{in}} \quad (33)$$

In this simulation, using Table 1 parameters, desired amplification was 10 times. It was realized by using value of R_{in} and R_f were 1 kΩ and 10 kΩ, respectively.

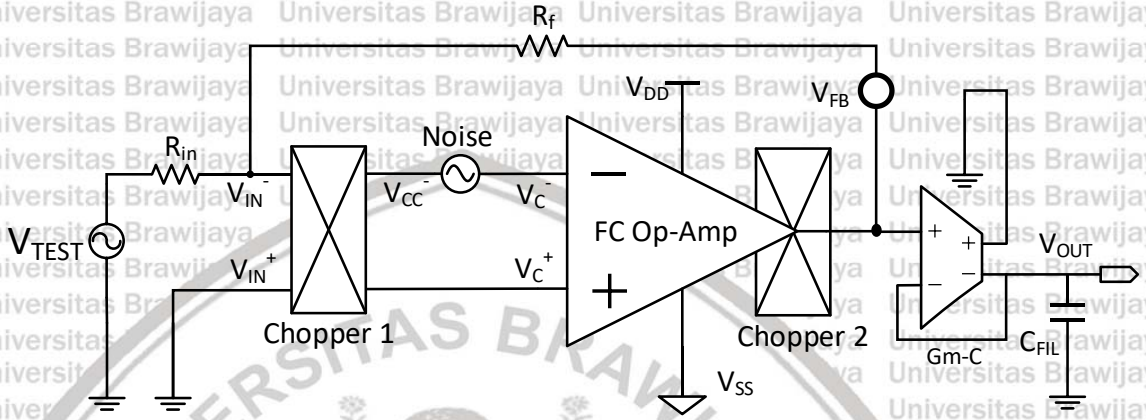

Figure 46. Implementation of proposed system into inverting amplifier

From the inverting amplifier, while -5 mV is used, 50 mV of output signal supposed to be gotten. In Figure 47, V_{OUT} and V_{IN} has a different polarity. Not only that, the desired amplification was nearly achieved, V_{OUT} value was around 47.8 mV in Figure 47. In addition, *1/f* noise which is added like Figure 46 was completely canceled. However, as shown in Figure 47, the wave form in point V_{FB} was not given any indication of demodulated input signal and modulated noise's separation.

Fast Fourier Transform (FFT) analysis technique from transient analysis is one technique to transform the response of transient analysis in time domain to frequency domain. The signal flows in FFT for each points (refers to Figure 46's V_{TEST}, V_{IN}^-, V_{CC}^-, V_C^-, V_{OUTh}, V_{FB}, V_{OUT}) are expressed in Figure 48 and Figure 49.Furthermore, using FFT, the comparison for amplification in point V_{TEST}, V_{FB} and V_{OUT} can be also analyzed (shown in Figure 50).

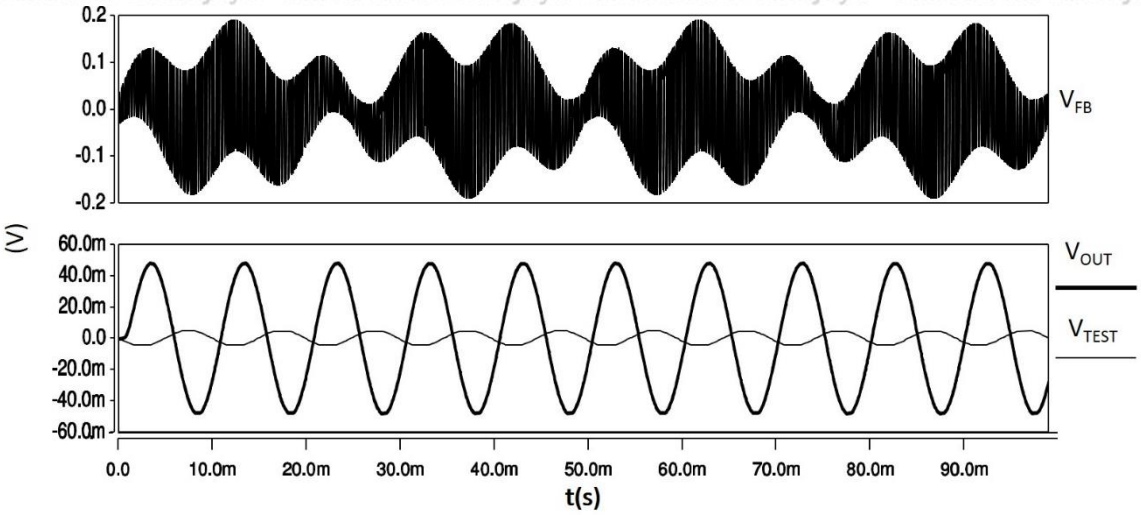

Figure 47. Simulation of inverting amplifier in transient analysis

As for Figure 48, the responses in frequency 1 Hz to 100 kHz is shown for point V_{TEST}, V_{IN}^-, V_{CC}^- and V_C^-. V_{TEST} has a magnitude -43.934 dB or 4.9 mV. V_{IN}^- is the junction of feedback which is placed after R_{in}. The parameters which are affected the signal in V_{IN}^- is R_{in} and R_f. R_{in} has a thermal noise and from feedback point (R_f), system will get modulated noise and thermal noise. As shown in Figure 48of V_{IN}^- point, these parameters made input signal suffered of voltage drop. In V_{IN}^- point, precisely on 10 kHz, it was shown the modulated noise given by feedback during the operation. This noise will be demodulated in 1st CST while the input signal was modulated into higher frequency (in this case 10 kHz).

The result of 1st CST was V_{CC}^- point. Because of noise demodulation, *1/f* noise is appeared in V_{CC}^- frequency domain even though on Figure 46, *1/f* noise was added after V_{CC}^-. Like mentioned previously, *1/f* noise is dominated low frequency noise and usually has a big effect among the other noises. This is proven by the rise in noise floor of V_{CC}^-. After V_{CC}^- signal input will be added with internal noise of amplifier (in this case *1/f* noise which is represented by 3 voltages in 20 Hz, 40 Hz and 60 Hz). V_C^- was the point to analyze this effect. However, in V_C^- the differences only appeared in slightly rise of noise floor.

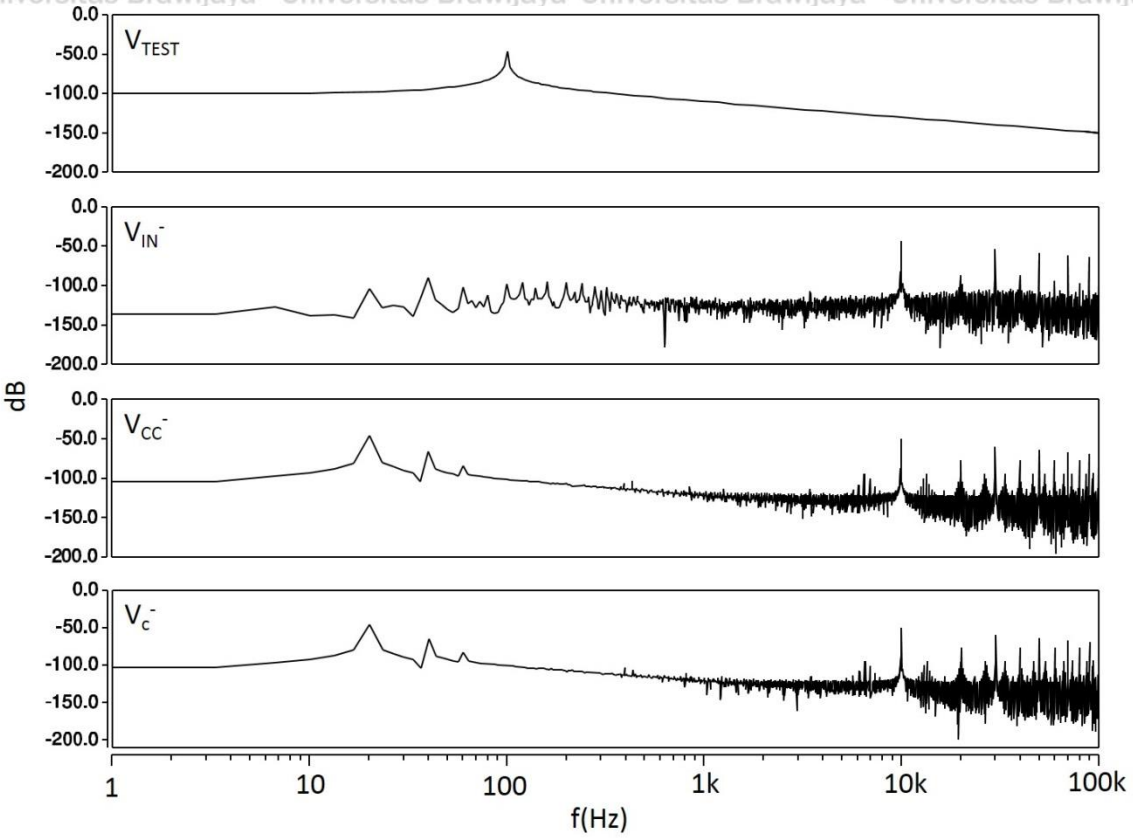

Figure 48. Signal's FFT (a)

Figure 49 represented of V_{OUTh}, V_{FB} and V_{OUT}. Point V_{OUTh} was the output place of 2nd CST. In V_{OUTh}, input signal and noise could be separated, they could be demodulated and modulated, respectively. This signal is amplified again using class AB common source before outputted into V_{FB} point and being feedback-ed. Signal input in 100Hz of this V_{FB} point was -23.939 dB or 49.215 mV. 10 times amplification was achieved.

Even though noise was already modulated into 10 kHz, it was still present in system. LPF was needed to be applied in order to remove this effect. Using 6th order Gm-C filter, noise can be canceled perfectly, in cost there will be slightly voltage drop. However, this voltage drop can be neglected. The value of 47.758 mV was acceptable.

The amplification in detail for Figure 46 was expressed into Figure 50. It was shown that from -43.934 dB was amplified into -24.201 dB. 9.697 times stands for their amplification. While in V_{FB} point (before LPF was added) the amplification

was 9.99 times. This is proving that proposed circuit will work well in canceled noises and amplified the input signal.

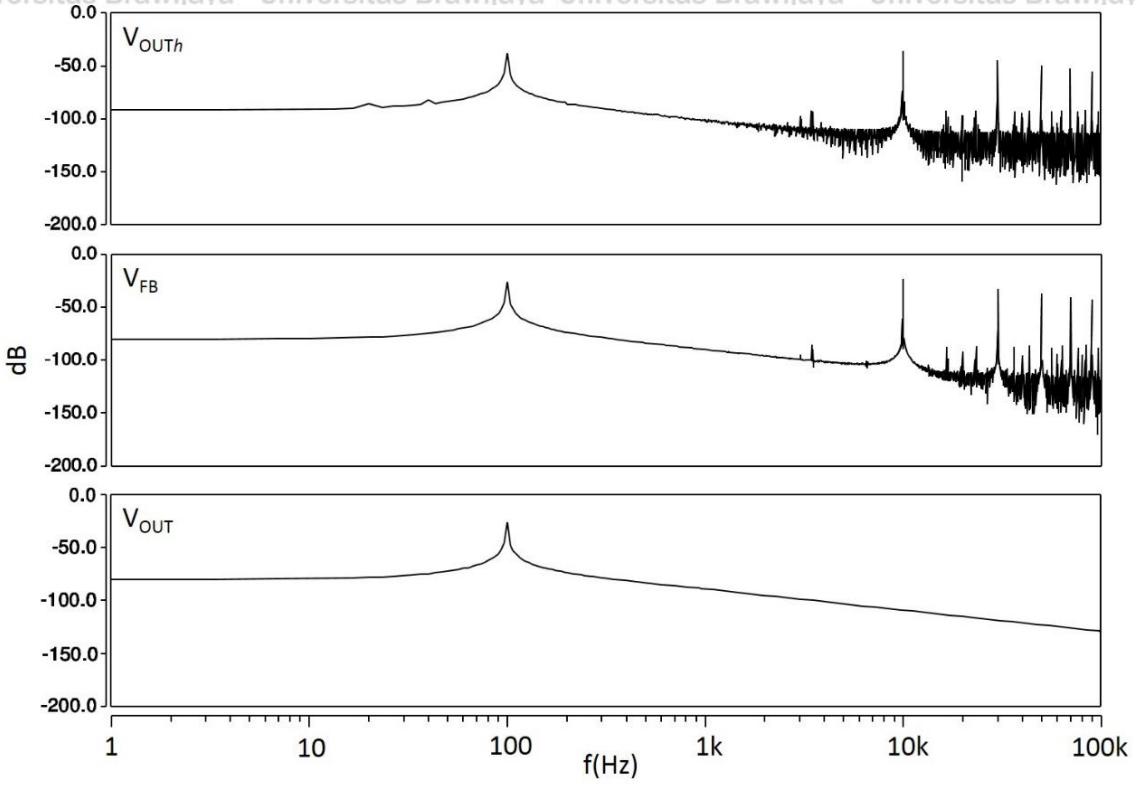

Figure 49. Signal's FFT (b)

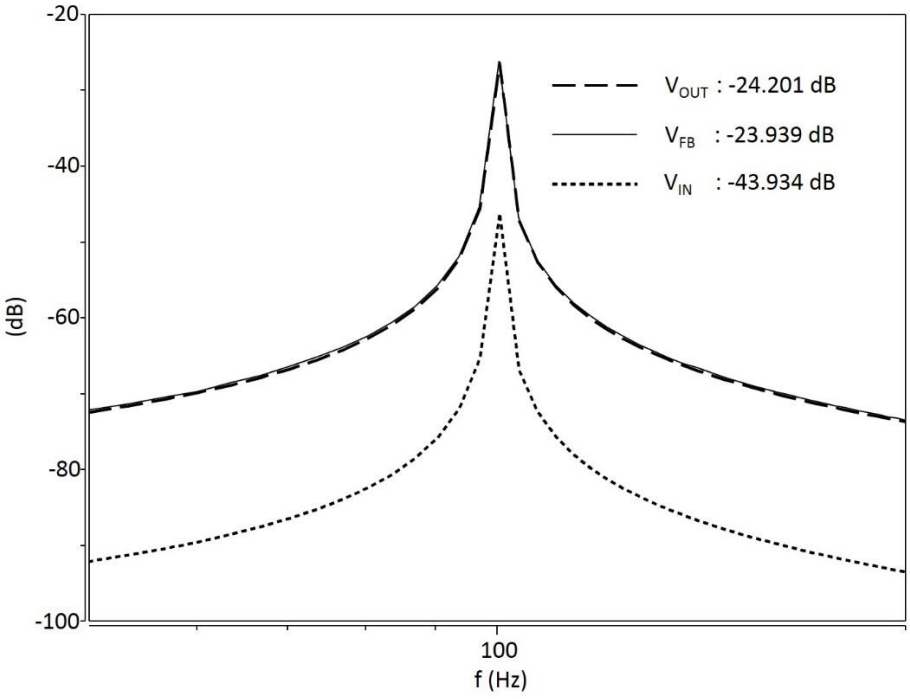

Figure 50. Amplification of proposed circuit

4.3 Different condition of new operational amplifier cell

It was mentioned in chapter 2that chopping frequency and filter frequency were set by using $f_{input} < f_{filter} < f_{chopping}$ conditions. Using V_{IN} on 100 Hz there will be several choices to determine frequency of chopping and filter. The examples of this choice are shown in Figure 51 and Figure 52.

Figure 51shows three chopping frequency under Table 1 condition of parameters. Using 1 kHz as filter frequency, chopping frequency is supposed to be larger. Using this as reason, 4 kHz, 10 kHz and 40 kHz is chosen as chopping frequency. As the result, larger frequency of chopping, smoother the FFT of Vout is. 10 kHz is chosen as chopping frequency in this proposed circuit due to it is not too far from 1 kHz and it already has a smooth result. Moreover 10 kHz had a same nose floor as 40 kHz.

As for Figure 52, it explains about the differences in 350 Hz and 1 kHz cut-off filter frequency. Using lower cut-off frequency (such as 350 Hz) will give lower noise floor, higher cut-off frequency will cost with higher noise floor too. However, in 350 Hz cut-off frequency, filter cannot cancel *1/f* noise after it is modulated into high frequency (10 kHz) even though it was using 6th order filter. Moreover, in 1 kHz cut-off frequency case, the output signal of it has better amplification than 350 Hz and *1/f* noise can be removed perfectly. Because of this, in this proposed circuit, 1 kHz cut-off frequency is used.

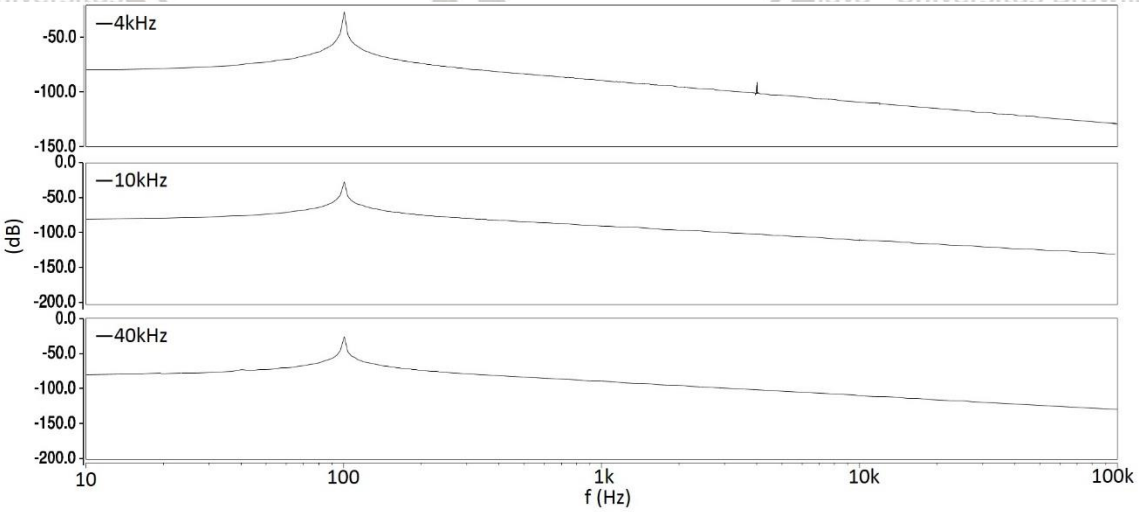

Figure 51. Condition of Vout using different chopping frequency

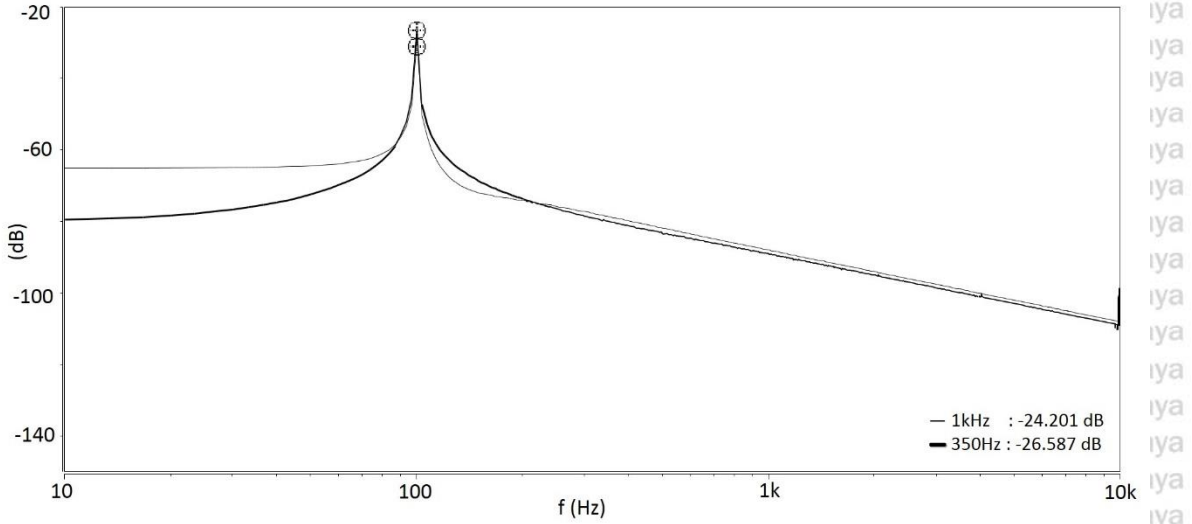

Figure 52. Condition of Vout using different filter frequency

4.4 Comparison of conventional IA and new proposed circuit

The new proposed circuit can be applied into anywhere as low *1/f* noise operational amplifier. This operational amplifier will reduce inside noise as reducing another noise from outside. Inverting amplifier circuit is one of fundamental example. In advance, this proposed circuit will be applied into conventional IA.

This conventional IA is one of basic FBDDA-DDA. If the processing in IA is succeeded, then it can reduce noises in DDA of FBDDA-DDA too. The condition of simulation is V_{IN}= ±1 mV on 100 Hz, in the respect to Figure 53. Using Table 4 as resistor parameters, IA will have 50.76 times amplification.

Table 4. Resistors of conventional IA

Item	Value
R1	22 kΩ
R2	10 kΩ
R3	10 kΩ
R4	47 kΩ

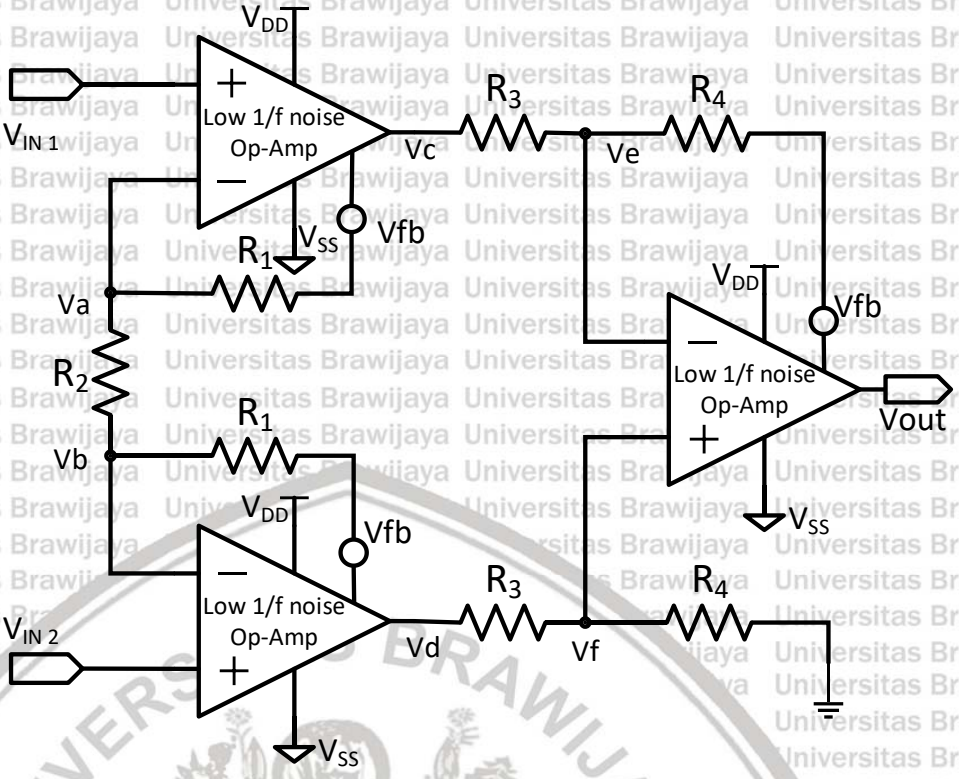

Figure 53. Application of new proposed circuit into conventional IA

Figure 54 and Figure 55 are the result of comparing both conventional IA and proposed circuit which is implemented into IA. The signal wave form in transient analysis is presented in V_C, V_D and V_{OUT} of Figure 54, while its input and output FFT are expressed in Figure 55.

Figure 54 explains that signal of conventional IA suffers of *1/f* noise effect while IA with proposed circuit can reduce *1/f* noise in each amplifier (refers to Figure 53). This statement is proven by using frequency domain analysis (FFT). In Figure 55, the output of conventional IA is dominated by *1/f* noise and the other noises, even though input signal in same magnitude (±1 mV). Moreover, the V_{OUT} magnitude of implementation proposed circuit in IA, is -24.231 dB or -47.59 mV from -50.76 mV amplification goal. In other hand, it has 6.25% of error.

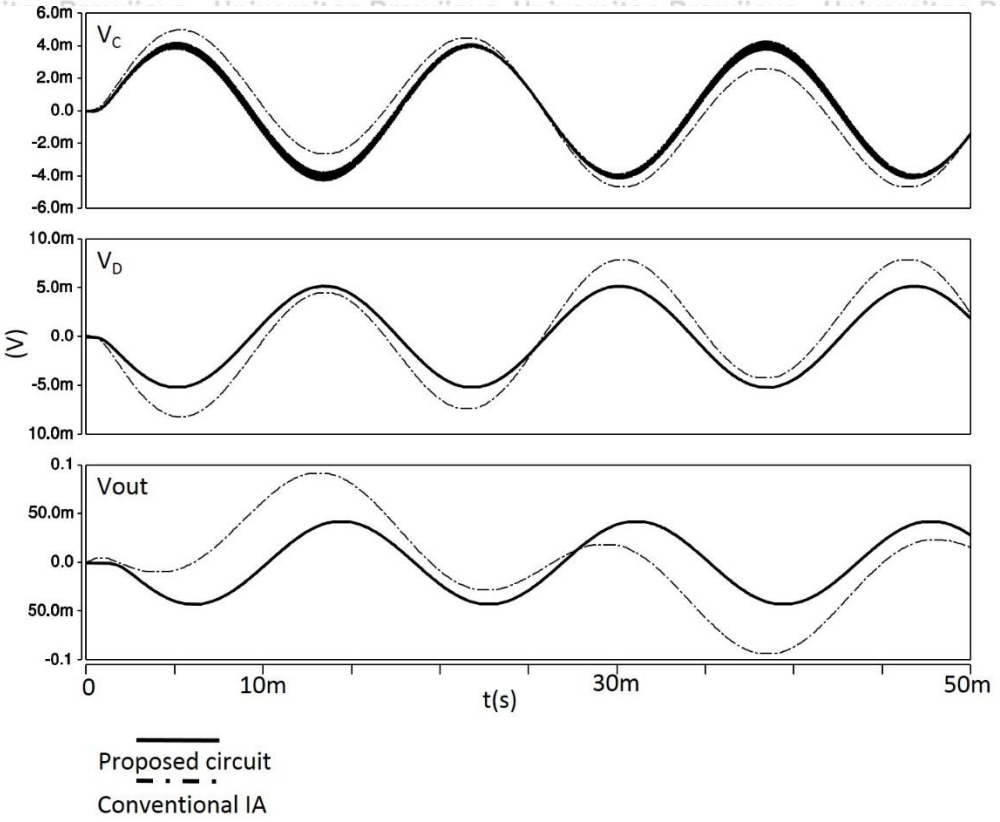

Figure 54. Comparison of conventional IA and proposed circuit

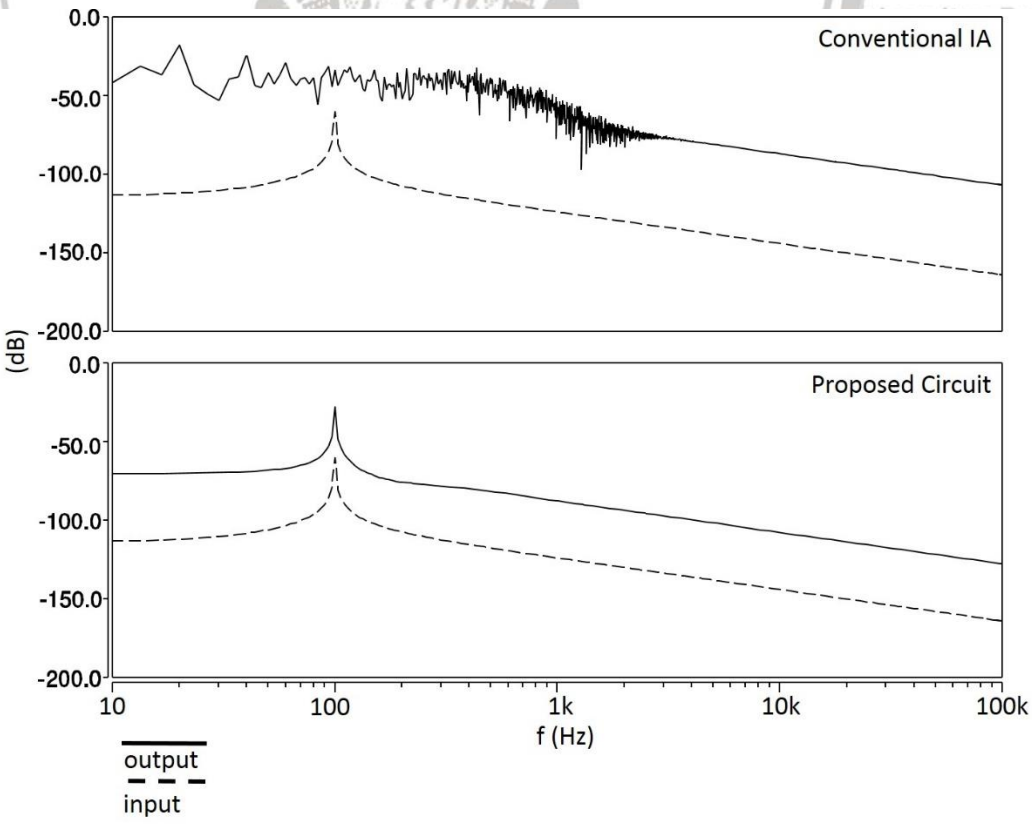

Figure 55. FFT of conventional IA and proposed circuit comparison

CHAPTER V
CONCLUSION AND FUTURE WORK

In this master thesis, the low *1/f* noise operational amplifier cell using chopper stabilization technique had been proposed. In this master thesis, how to apply the chopper switch to the single-ended-output was presented. The proposed circuit was designed by using by Phenitec Semiconductor 3-Metal 0.6 µm CMOS process and evaluated by using HSPICE. According to the design and simulation results the performance of the circuits could be summarized as follows.

1. *1/f* noise could be separated with input signal and removed perfectly at the output node.
2. DC gain, unity gain frequency, and phase margin of the proposed operational amplifier were 126.56 dB, 3.023 MHz, and 58.018^{o}. They are enough value for general use and applications.
3. The application circuits such as inverted amplifier and instrumentation amplifier are designed and evaluated. The circuits operated well as theory.

The proposed operational amplifier can be applied to various application circuits easily by replacing the operational amplifier in the application circuit with the proposed circuit.

It is very useful for low frequency application such as sensor interface circuits for healthcare and medical devices.

The proposed circuit is relatively high power consumption and occupied large chip area compared with conventional one because some circuits are added for chopper stabilization technique. These are the remaining research and will be done in near future.

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