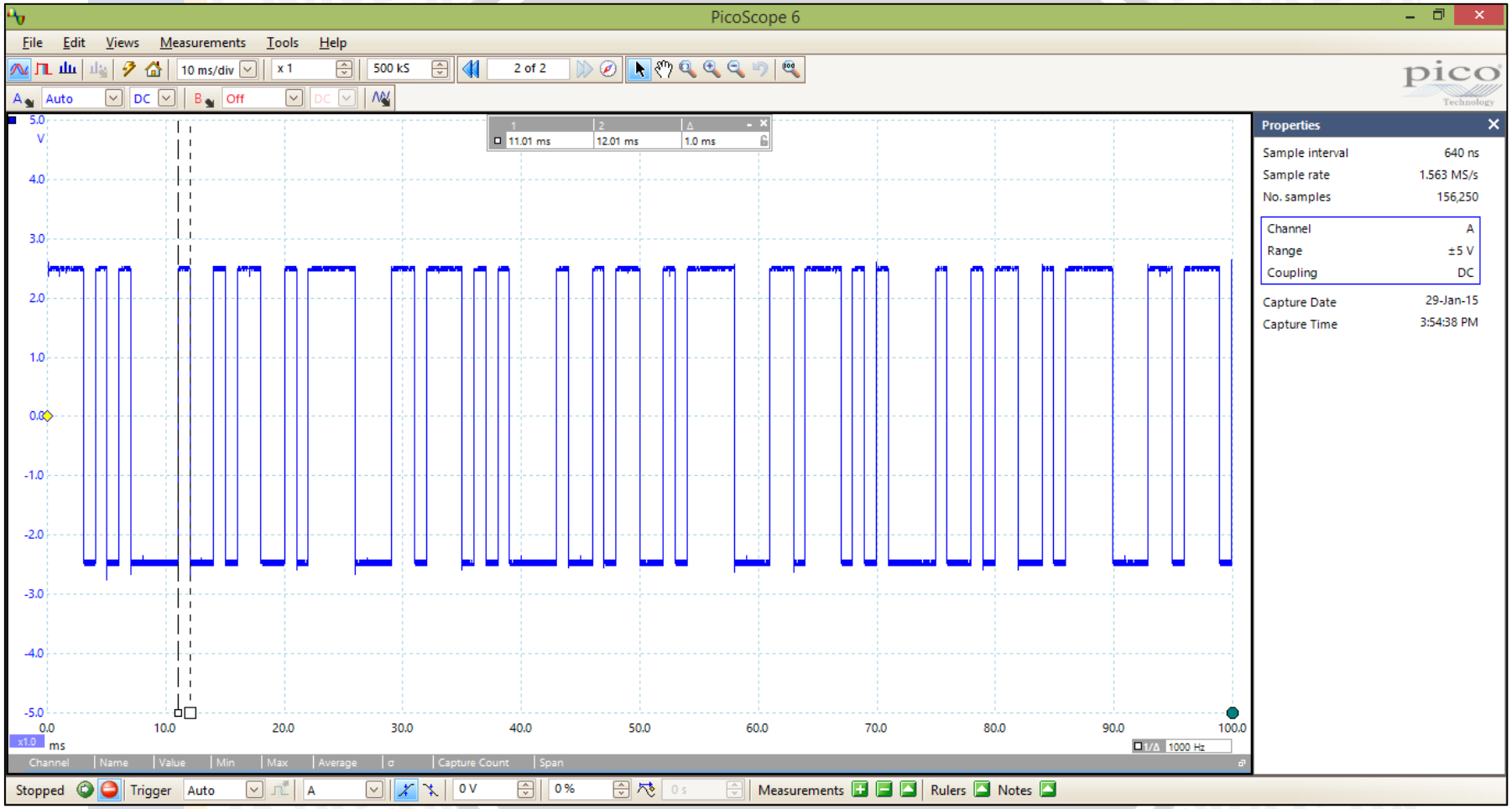
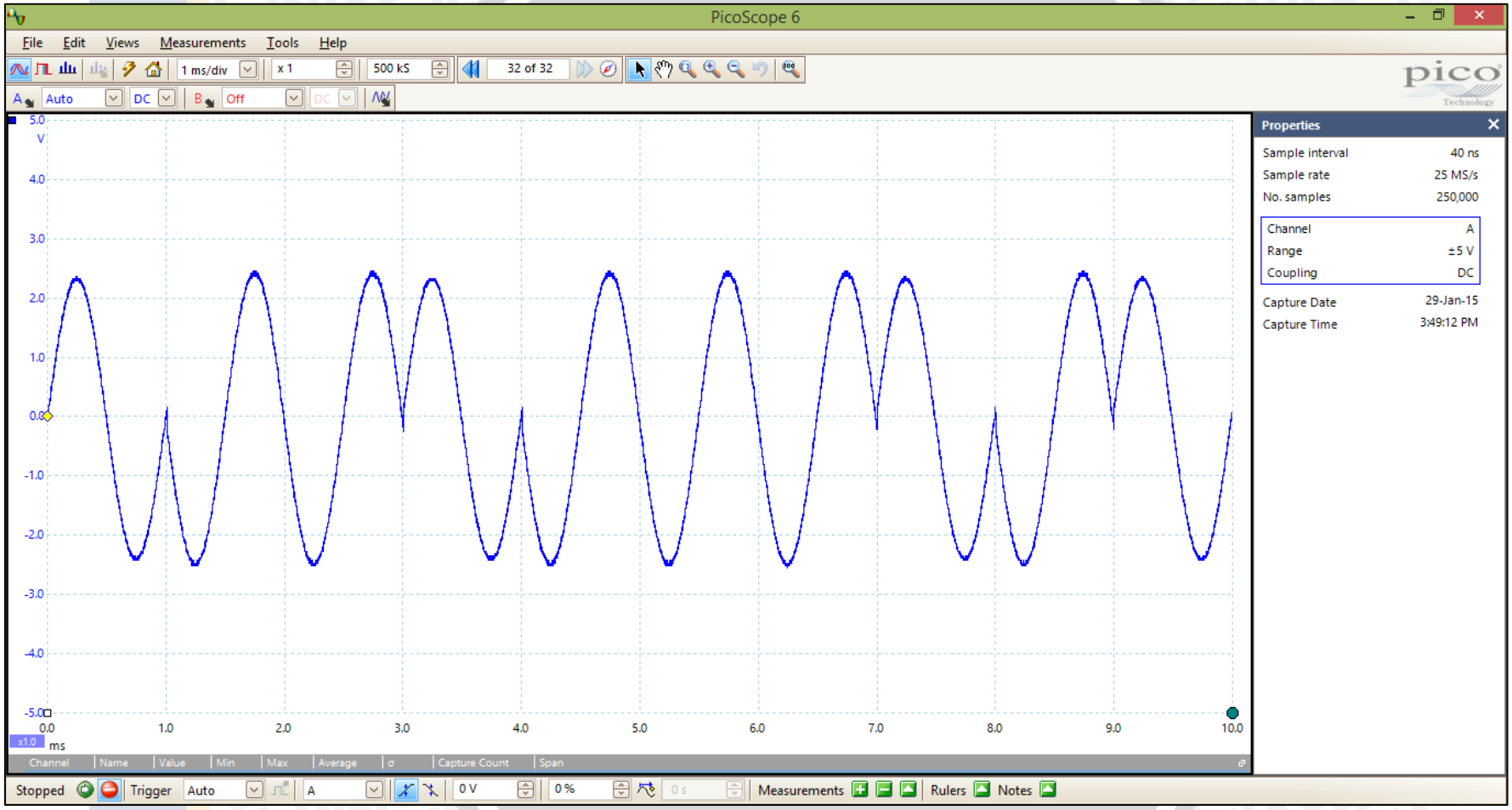
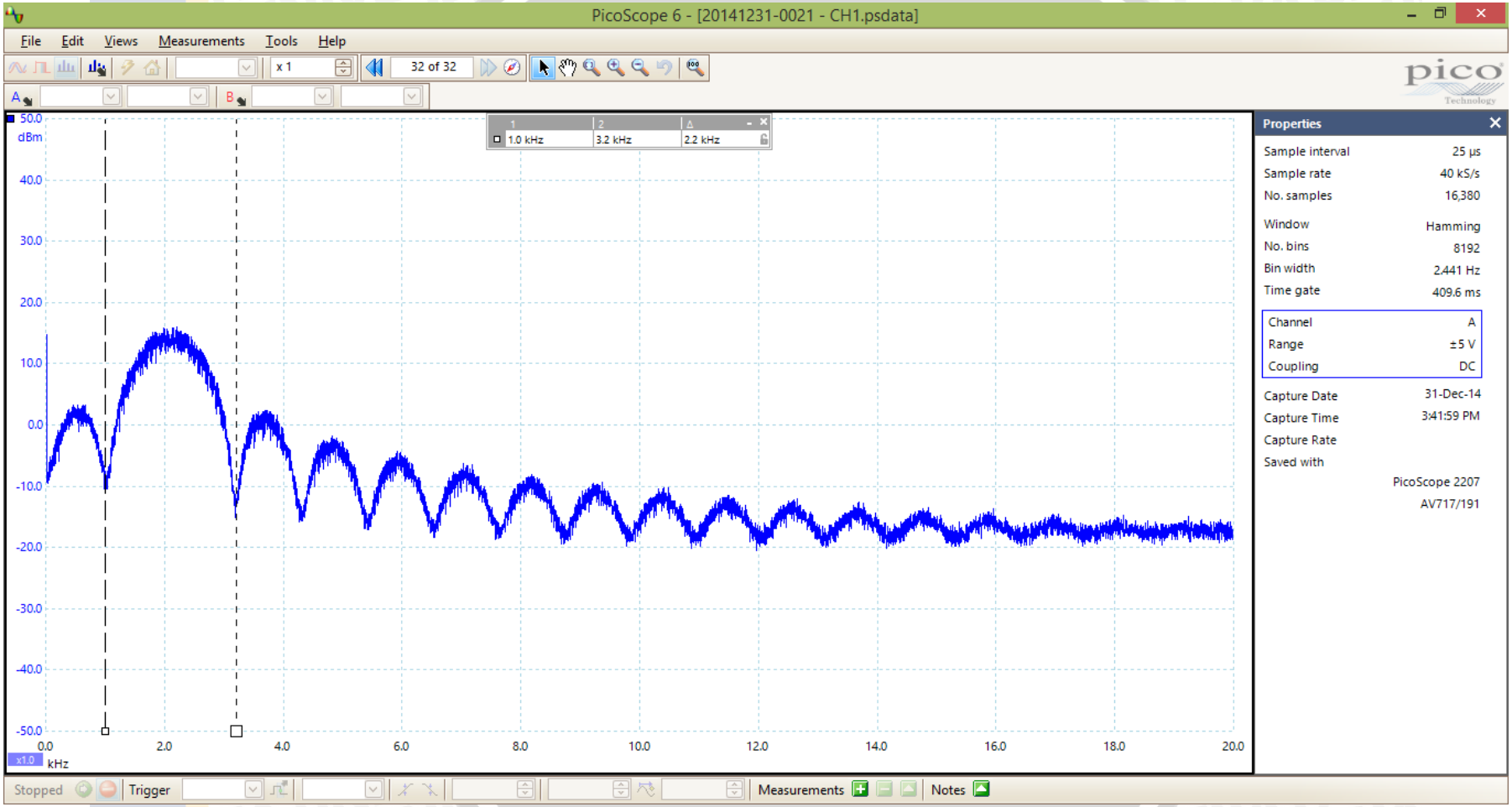
Lampiran 1 Data Acak oleh *Sequence Generator* dengan Periode 1 ms.



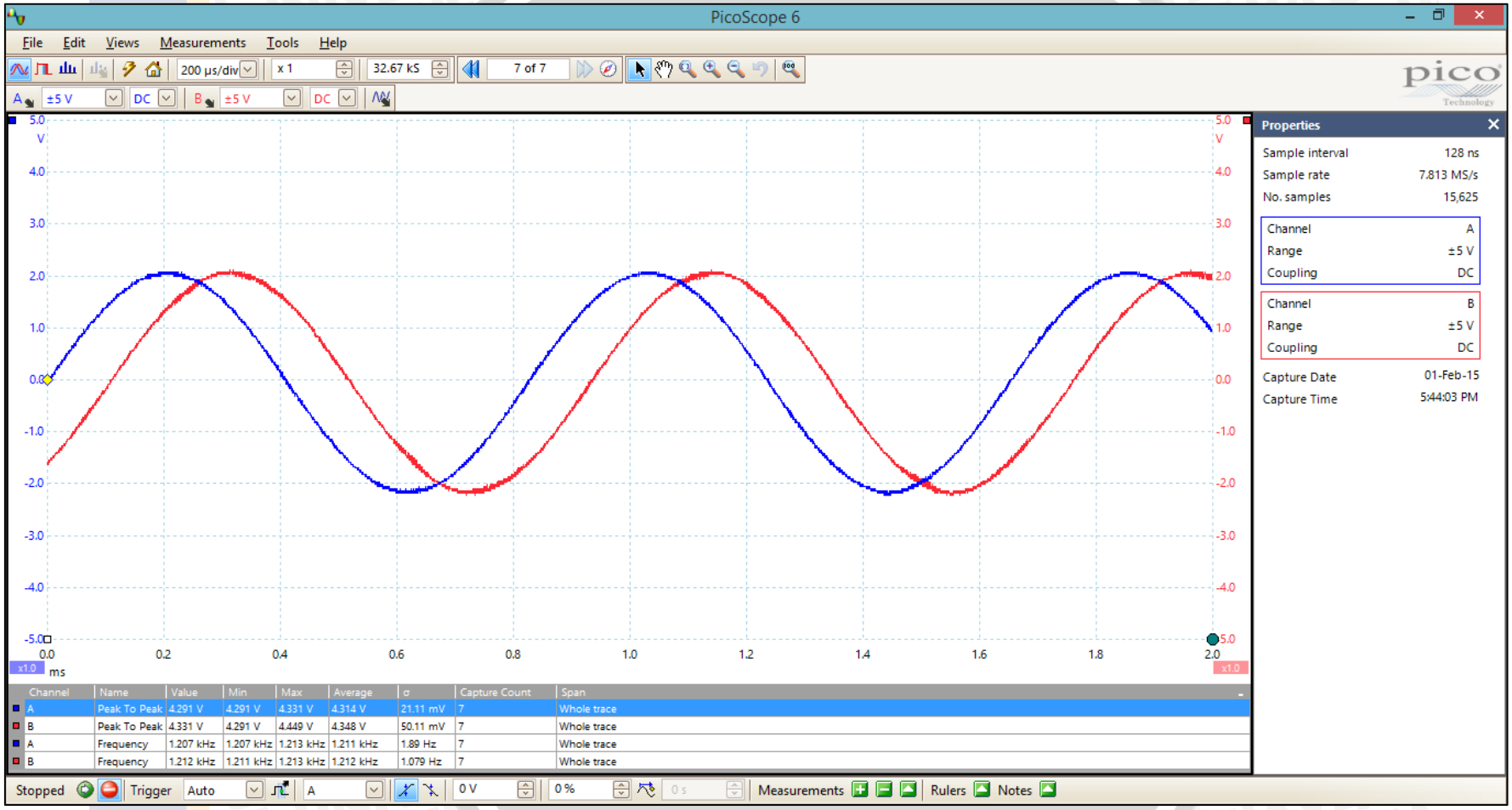
Lampiran 2 Sinyal BPSK Kanal Pertama dengan



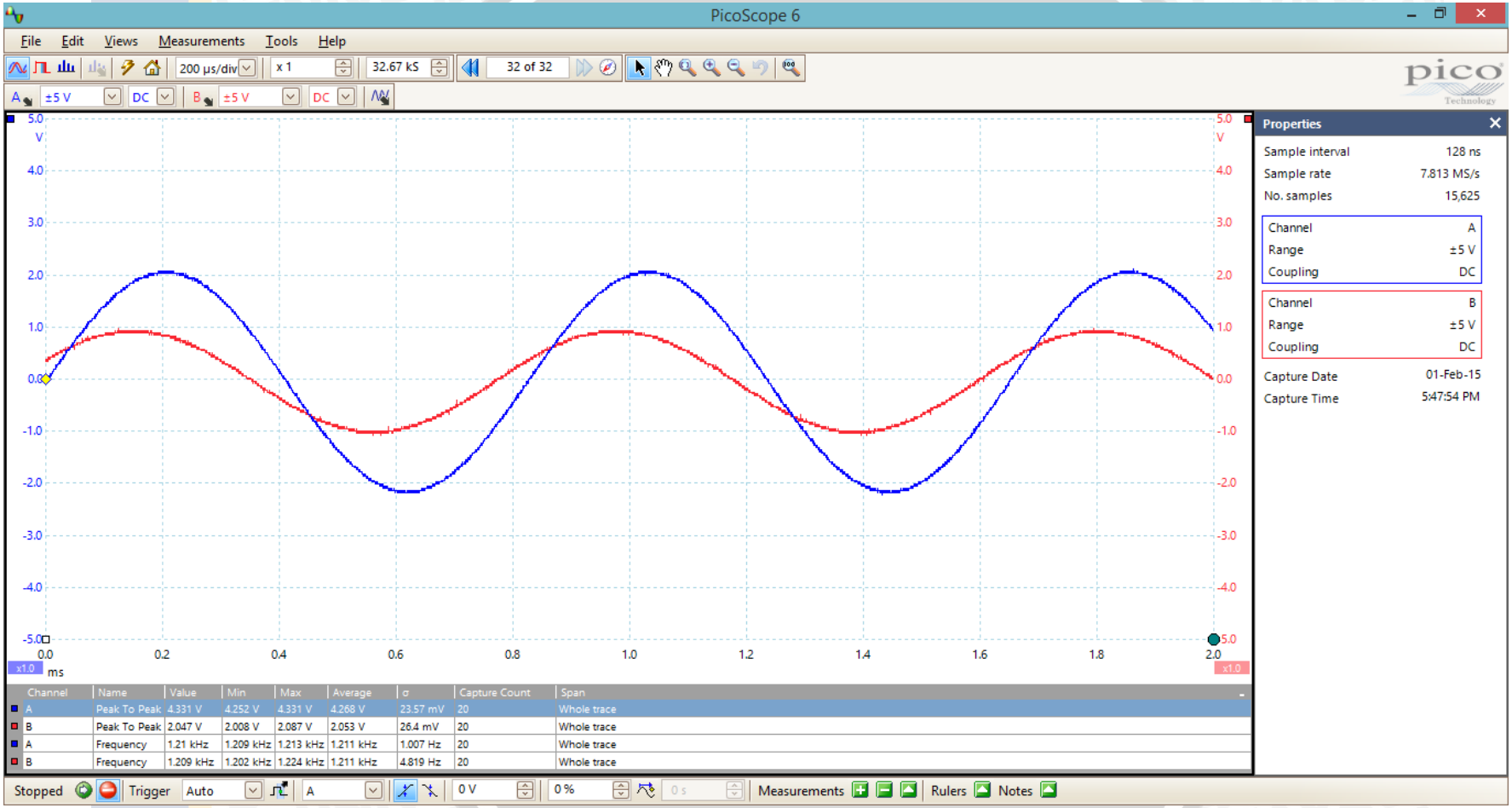
Lampiran 3 Penentuan Frekuensi *Subcarrier* Kanal Pertama dan Ketiga.



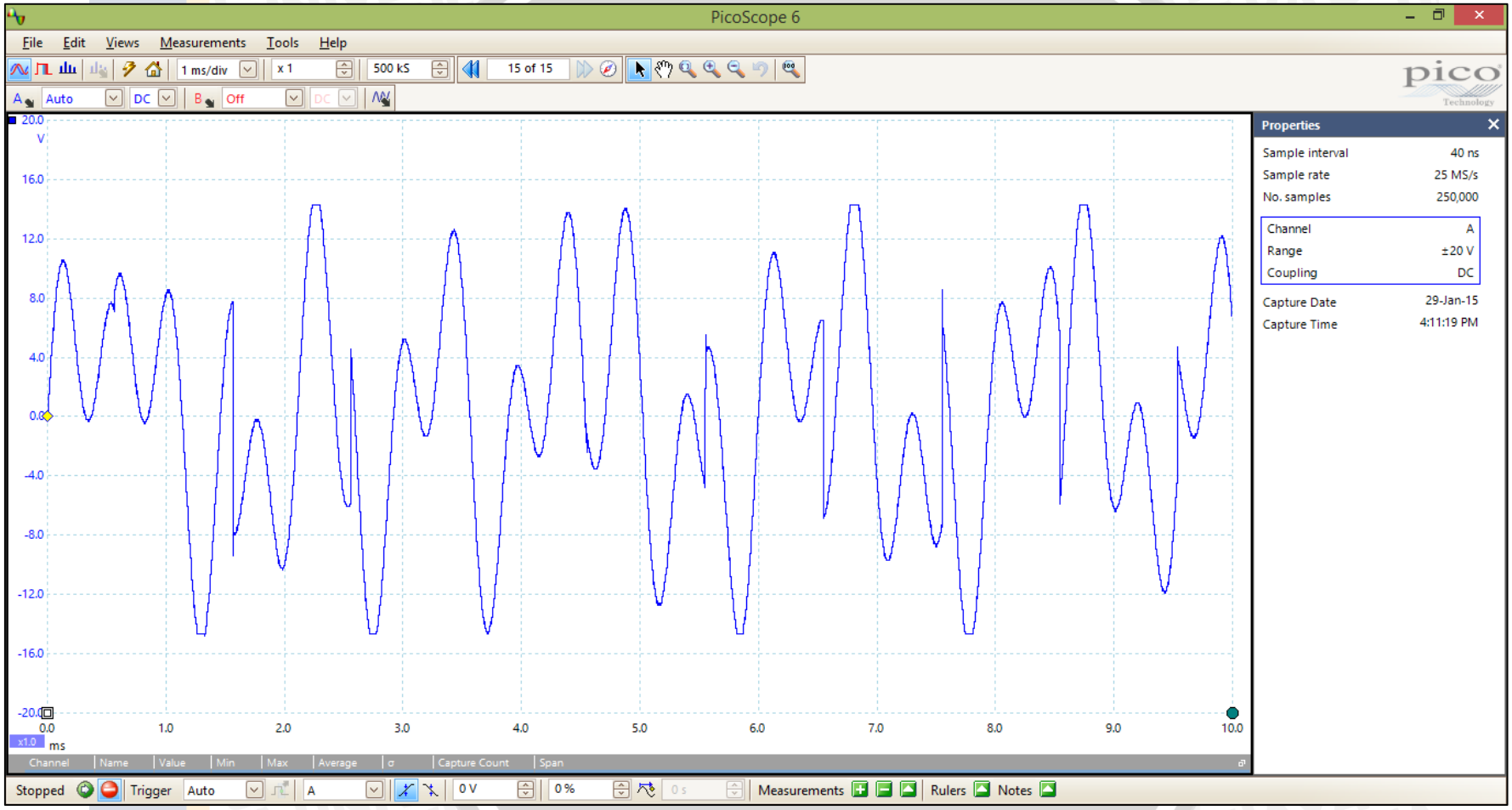
Lampiran 4 Tegangan Sinyal Masukan (Biru) dan Keluaran (Merah) Filter yang Bernilai Sama.



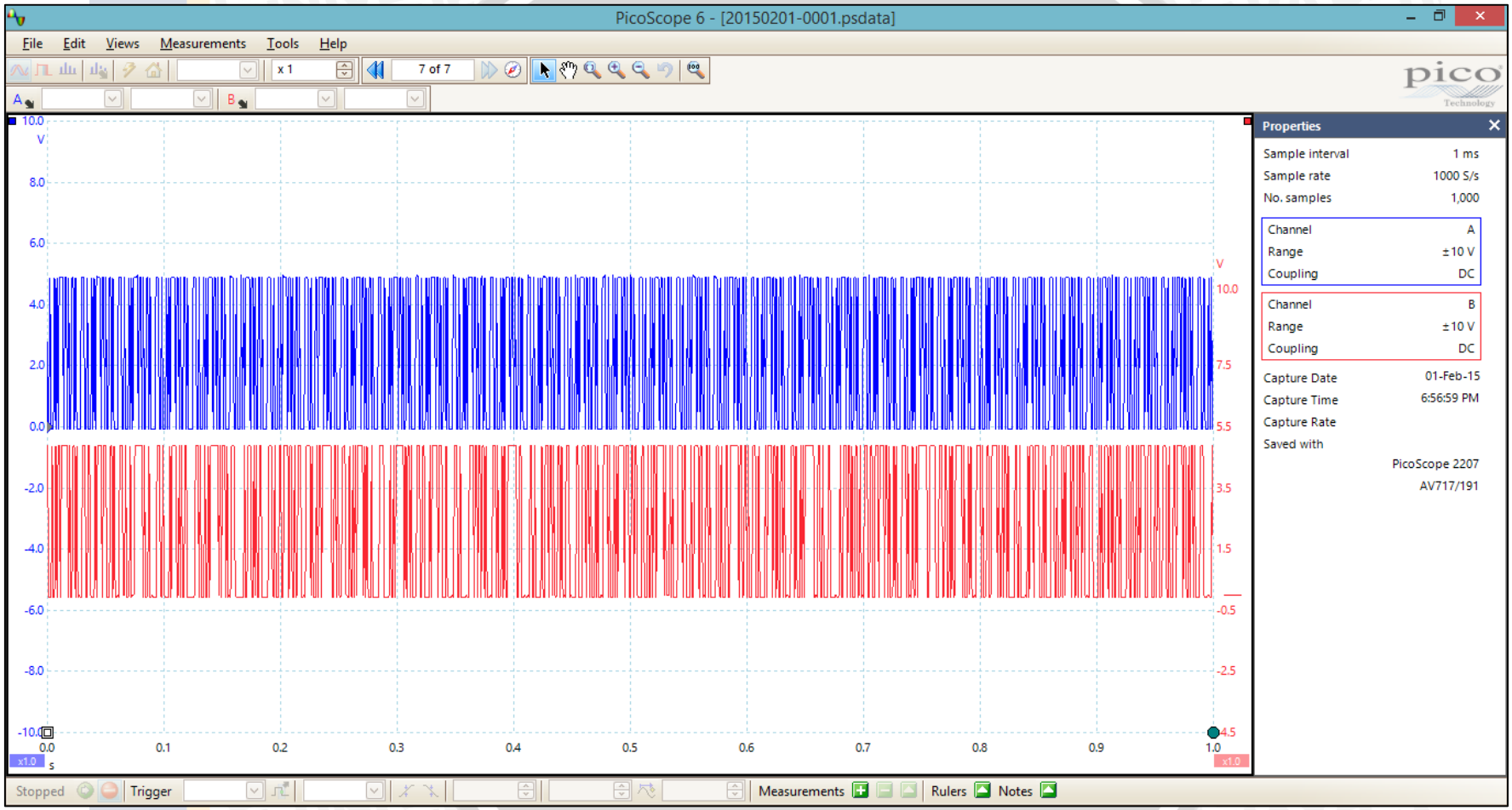
Lampiran 5 Sinyal dengan *Cut-Off* 1,2 kHz.



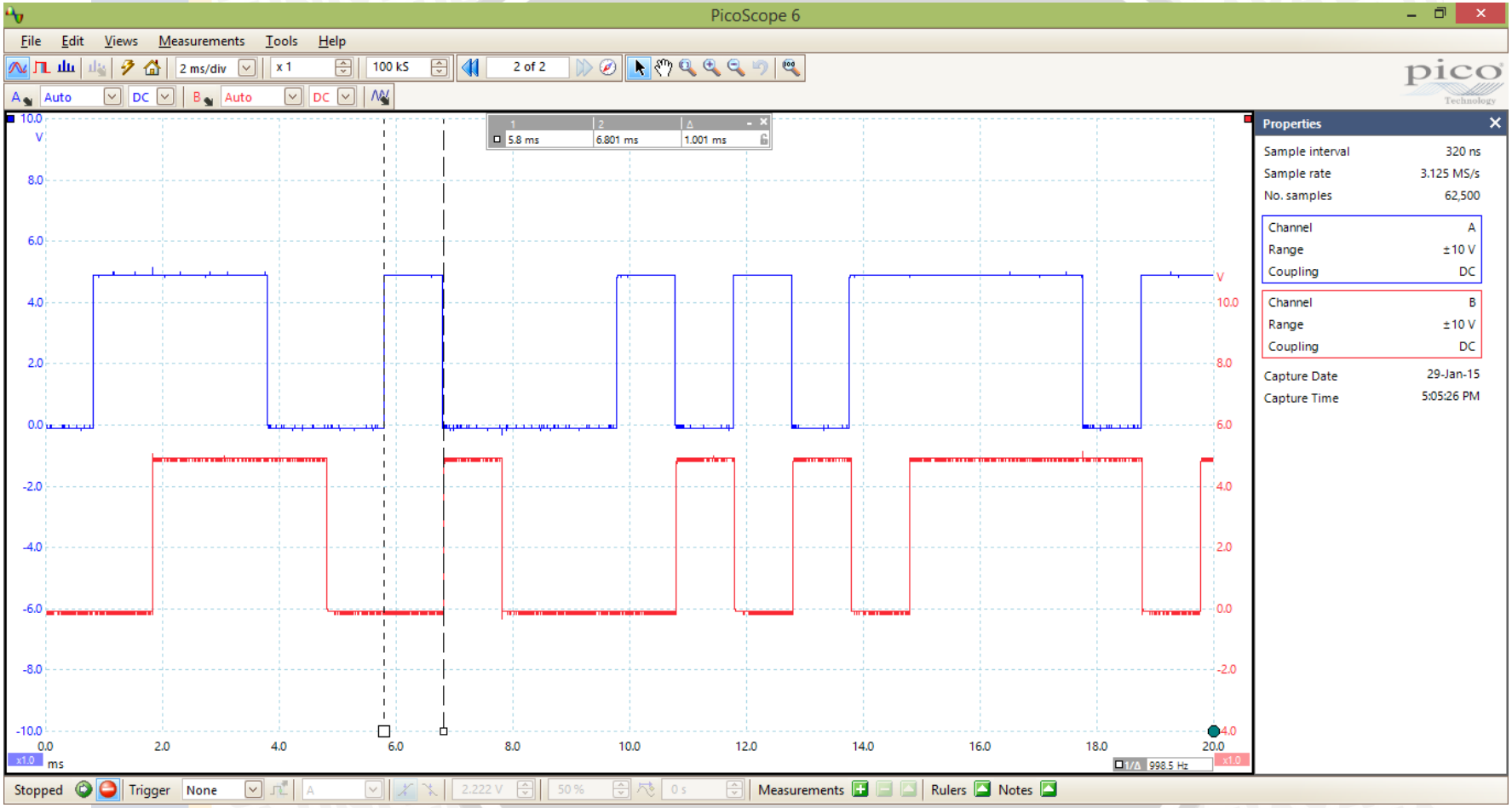
Lampiran 6 Sinyal Keluaran OFDM.



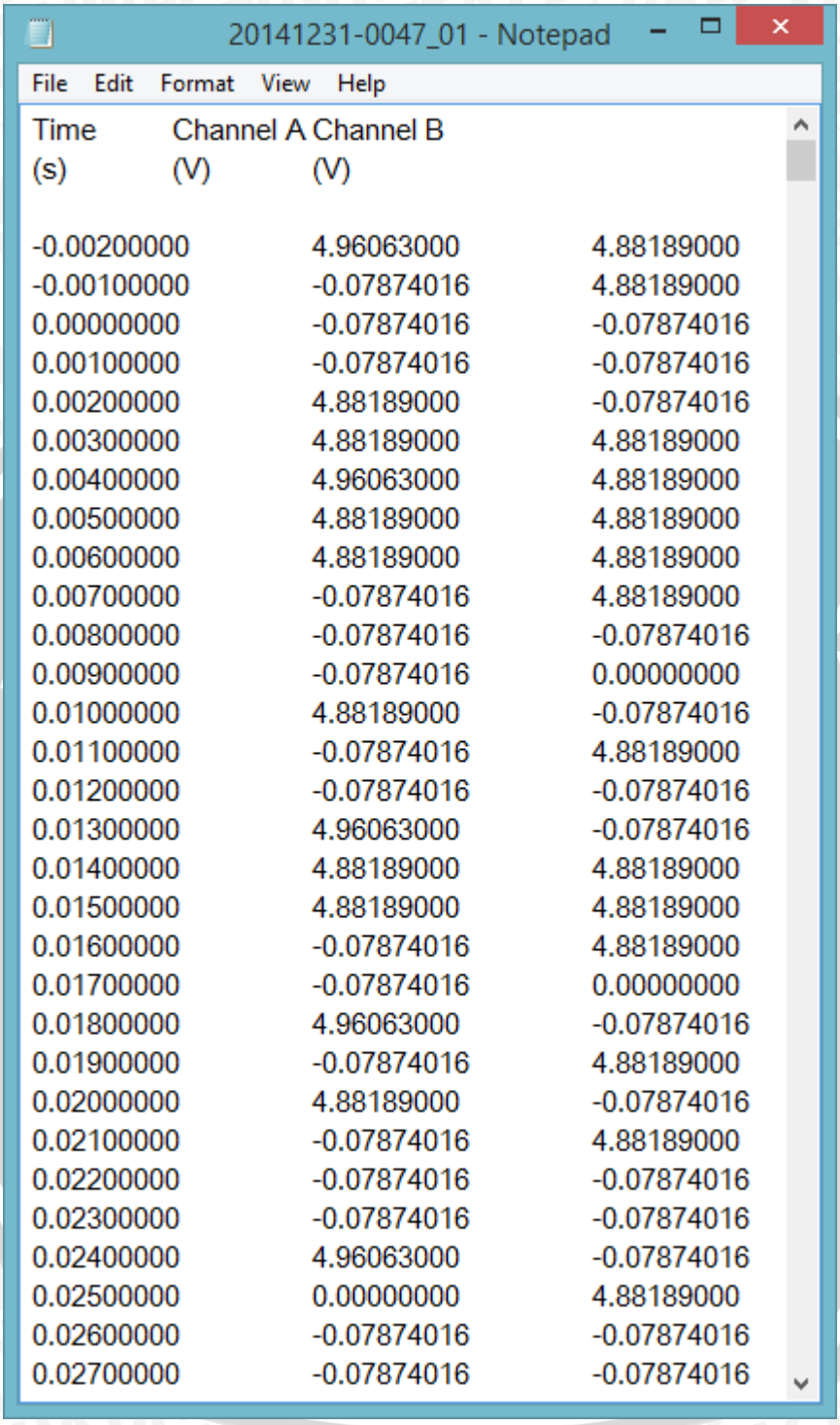
Lampiran 7 Data yang Dikirim (Biru) dan Diterima (Merah) dengan Periode Pengamatan 1 Detik dengan 7 Sampel.



Lampiran 8 *Delay* yang Terjadi pada Sistem OFDM sebesar 1 ms



Lampiran 9 Data yang Dikirimkan dan Diterima dalam Bentuk Teks.



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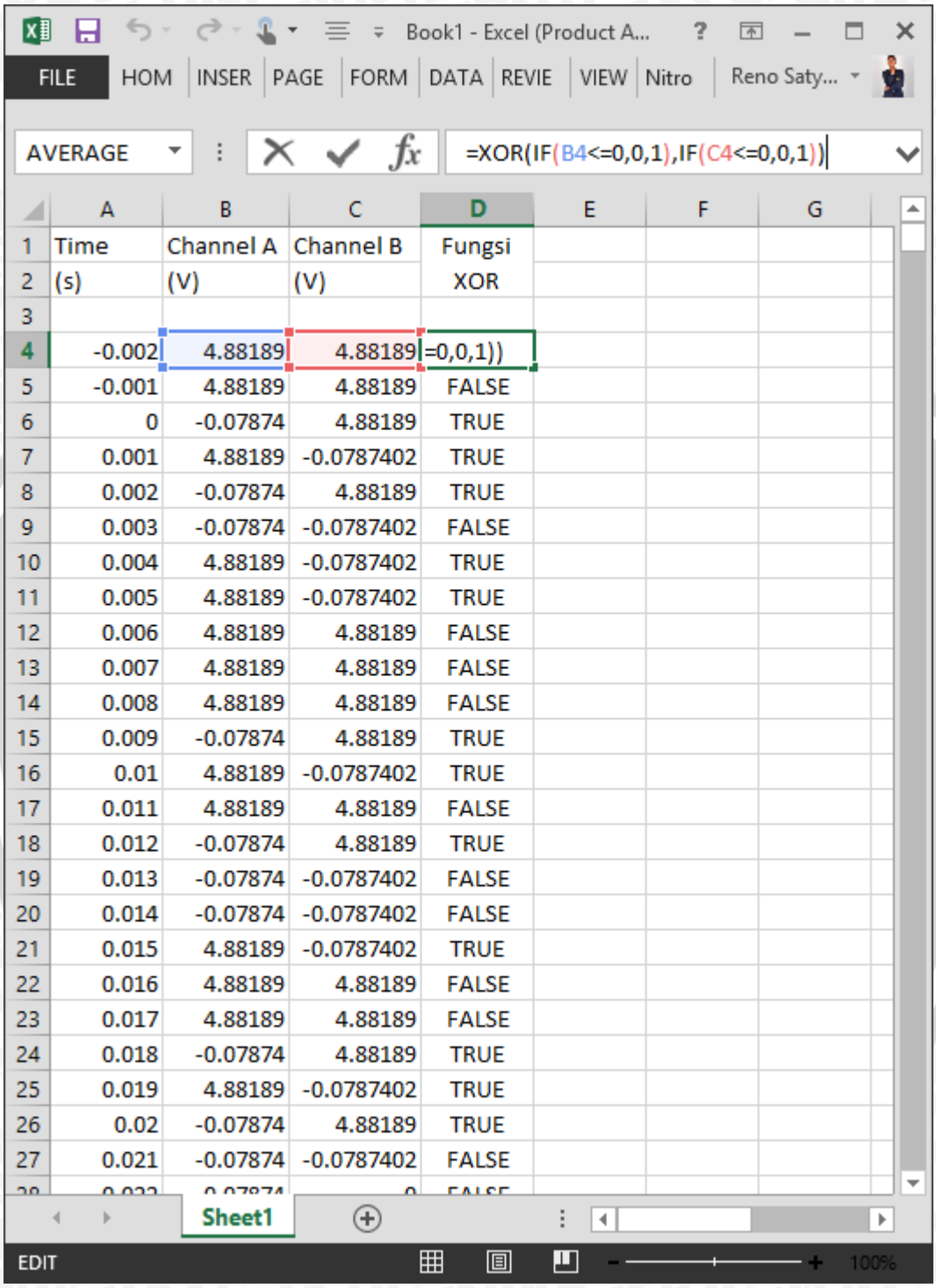
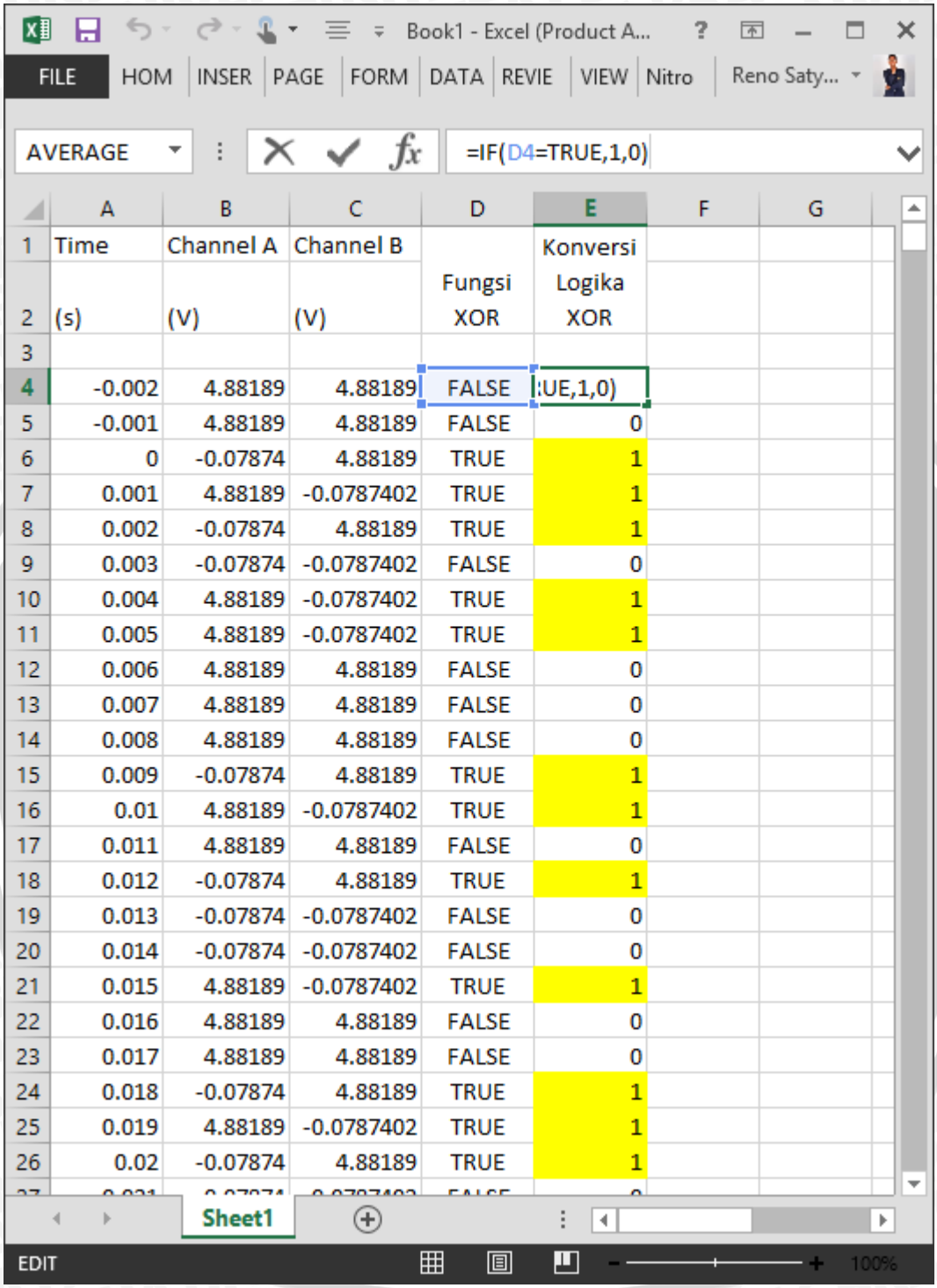
Time (s)	Channel A (V)	Channel B (V)
-0.00200000	4.96063000	4.88189000
-0.00100000	-0.07874016	4.88189000
0.00000000	-0.07874016	-0.07874016
0.00100000	-0.07874016	-0.07874016
0.00200000	4.88189000	-0.07874016
0.00300000	4.88189000	4.88189000
0.00400000	4.96063000	4.88189000
0.00500000	4.88189000	4.88189000
0.00600000	4.88189000	4.88189000
0.00700000	-0.07874016	4.88189000
0.00800000	-0.07874016	-0.07874016
0.00900000	-0.07874016	0.00000000
0.01000000	4.88189000	-0.07874016
0.01100000	-0.07874016	4.88189000
0.01200000	-0.07874016	-0.07874016
0.01300000	4.96063000	-0.07874016
0.01400000	4.88189000	4.88189000
0.01500000	4.88189000	4.88189000
0.01600000	-0.07874016	4.88189000
0.01700000	-0.07874016	0.00000000
0.01800000	4.96063000	-0.07874016
0.01900000	-0.07874016	4.88189000
0.02000000	4.88189000	-0.07874016
0.02100000	-0.07874016	4.88189000
0.02200000	-0.07874016	-0.07874016
0.02300000	-0.07874016	-0.07874016
0.02400000	4.96063000	-0.07874016
0.02500000	0.00000000	4.88189000
0.02600000	-0.07874016	-0.07874016
0.02700000	-0.07874016	-0.07874016

Lampiran 10 Fungsi *XOR* Antara Data yang Dikirim (*Channel* A) dengan yang Diterima (*Channel* B).



	A	B	C	D
1	Time	Channel A	Channel B	Fungsi
2	(s)	(V)	(V)	XOR
3				
4	-0.002	4.88189	4.88189	=0,0,1))
5	-0.001	4.88189	4.88189	FALSE
6	0	-0.07874	4.88189	TRUE
7	0.001	4.88189	-0.0787402	TRUE
8	0.002	-0.07874	4.88189	TRUE
9	0.003	-0.07874	-0.0787402	FALSE
10	0.004	4.88189	-0.0787402	TRUE
11	0.005	4.88189	-0.0787402	TRUE
12	0.006	4.88189	4.88189	FALSE
13	0.007	4.88189	4.88189	FALSE
14	0.008	4.88189	4.88189	FALSE
15	0.009	-0.07874	4.88189	TRUE
16	0.01	4.88189	-0.0787402	TRUE
17	0.011	4.88189	4.88189	FALSE
18	0.012	-0.07874	4.88189	TRUE
19	0.013	-0.07874	-0.0787402	FALSE
20	0.014	-0.07874	-0.0787402	FALSE
21	0.015	4.88189	-0.0787402	TRUE
22	0.016	4.88189	4.88189	FALSE
23	0.017	4.88189	4.88189	FALSE
24	0.018	-0.07874	4.88189	TRUE
25	0.019	4.88189	-0.0787402	TRUE
26	0.02	-0.07874	4.88189	TRUE
27	0.021	-0.07874	-0.0787402	FALSE

Lampiran 11 Pengonversian Logika pada Fungsi *XOR*.



Book1 - Excel (Product A...

FILE | HOM | INSER | PAGE | FORM | DATA | REVIE | VIEW | Nitro | Reno Saty...

AVERAGE | =IF(D4=TRUE,1,0)

	A	B	C	D	E	F	G
1	Time	Channel A	Channel B		Konversi		
2	(s)	(V)	(V)	Fungsi XOR	Logika XOR		
3							
4	-0.002	4.88189	4.88189	FALSE	:UE,1,0)		
5	-0.001	4.88189	4.88189	FALSE	0		
6	0	-0.07874	4.88189	TRUE	1		
7	0.001	4.88189	-0.0787402	TRUE	1		
8	0.002	-0.07874	4.88189	TRUE	1		
9	0.003	-0.07874	-0.0787402	FALSE	0		
10	0.004	4.88189	-0.0787402	TRUE	1		
11	0.005	4.88189	-0.0787402	TRUE	1		
12	0.006	4.88189	4.88189	FALSE	0		
13	0.007	4.88189	4.88189	FALSE	0		
14	0.008	4.88189	4.88189	FALSE	0		
15	0.009	-0.07874	4.88189	TRUE	1		
16	0.01	4.88189	-0.0787402	TRUE	1		
17	0.011	4.88189	4.88189	FALSE	0		
18	0.012	-0.07874	4.88189	TRUE	1		
19	0.013	-0.07874	-0.0787402	FALSE	0		
20	0.014	-0.07874	-0.0787402	FALSE	0		
21	0.015	4.88189	-0.0787402	TRUE	1		
22	0.016	4.88189	4.88189	FALSE	0		
23	0.017	4.88189	4.88189	FALSE	0		
24	0.018	-0.07874	4.88189	TRUE	1		
25	0.019	4.88189	-0.0787402	TRUE	1		
26	0.02	-0.07874	4.88189	TRUE	1		

Sheet1

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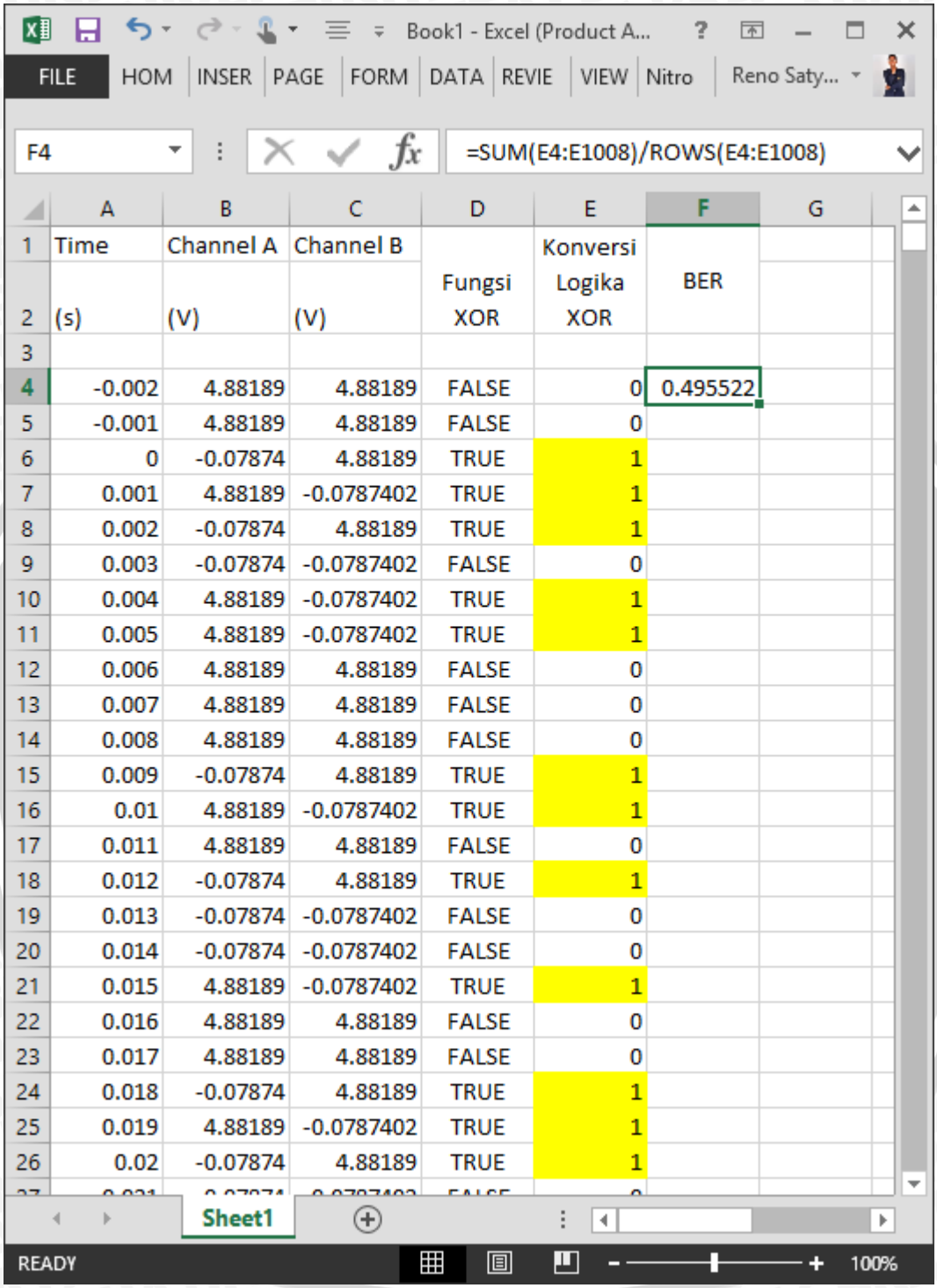
Lampiran 12 Perhitungan BER.



Book1 - Excel (Product A...

FILE | HOM | INSER | PAGE | FORM | DATA | REVIE | VIEW | Nitro | Reno Saty...

F4 =SUM(E4:E1008)/ROWS(E4:E1008)

	A	B	C	D	E	F	G
1	Time	Channel A	Channel B		Konversi		
2	(s)	(V)	(V)	Fungsi XOR	Logika XOR	BER	
3							
4	-0.002	4.88189	4.88189	FALSE	0	0.495522	
5	-0.001	4.88189	4.88189	FALSE	0		
6	0	-0.07874	4.88189	TRUE	1		
7	0.001	4.88189	-0.0787402	TRUE	1		
8	0.002	-0.07874	4.88189	TRUE	1		
9	0.003	-0.07874	-0.0787402	FALSE	0		
10	0.004	4.88189	-0.0787402	TRUE	1		
11	0.005	4.88189	-0.0787402	TRUE	1		
12	0.006	4.88189	4.88189	FALSE	0		
13	0.007	4.88189	4.88189	FALSE	0		
14	0.008	4.88189	4.88189	FALSE	0		
15	0.009	-0.07874	4.88189	TRUE	1		
16	0.01	4.88189	-0.0787402	TRUE	1		
17	0.011	4.88189	4.88189	FALSE	0		
18	0.012	-0.07874	4.88189	TRUE	1		
19	0.013	-0.07874	-0.0787402	FALSE	0		
20	0.014	-0.07874	-0.0787402	FALSE	0		
21	0.015	4.88189	-0.0787402	TRUE	1		
22	0.016	4.88189	4.88189	FALSE	0		
23	0.017	4.88189	4.88189	FALSE	0		
24	0.018	-0.07874	4.88189	TRUE	1		
25	0.019	4.88189	-0.0787402	TRUE	1		
26	0.02	-0.07874	4.88189	TRUE	1		

Sheet1

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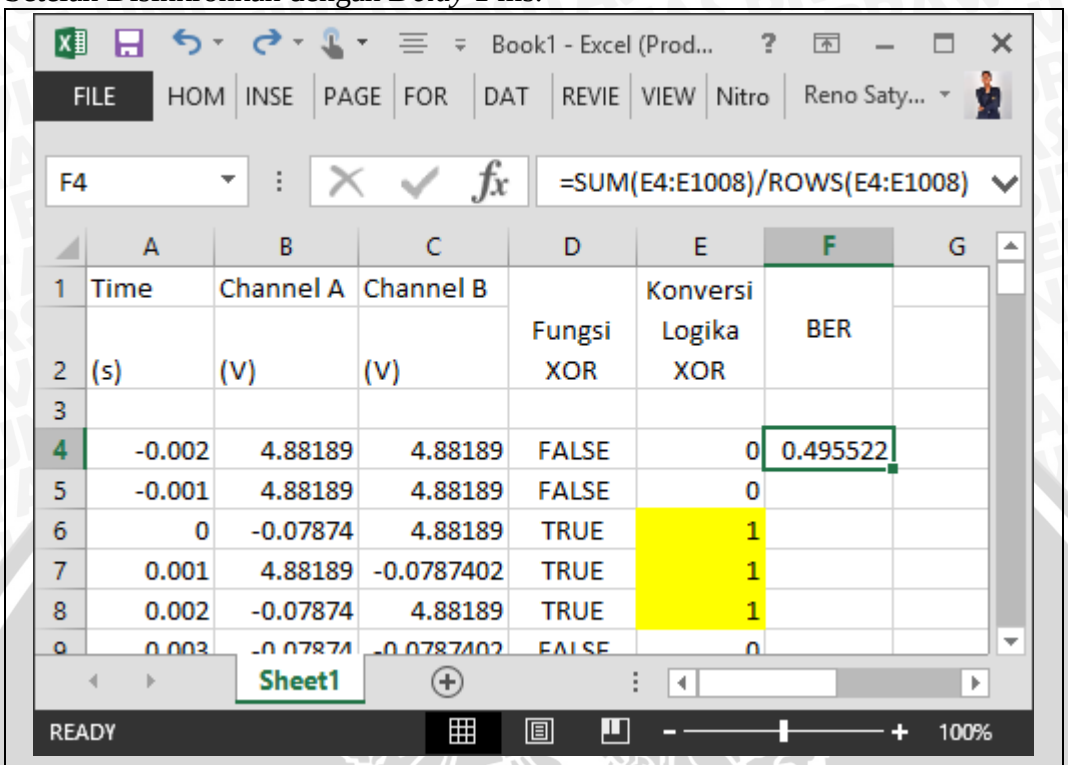
Lampiran 13 Analisis Sinkronisasi BER: (a) Sebelum Data disinkronkan dan (b) Setelah Disinkronkan dengan *Delay* 1 ms.



Book1 - Excel (Prod...

FILE | HOM | INSE | PAGE | FOR | DAT | REVIE | VIEW | Nitro | Reno Saty...

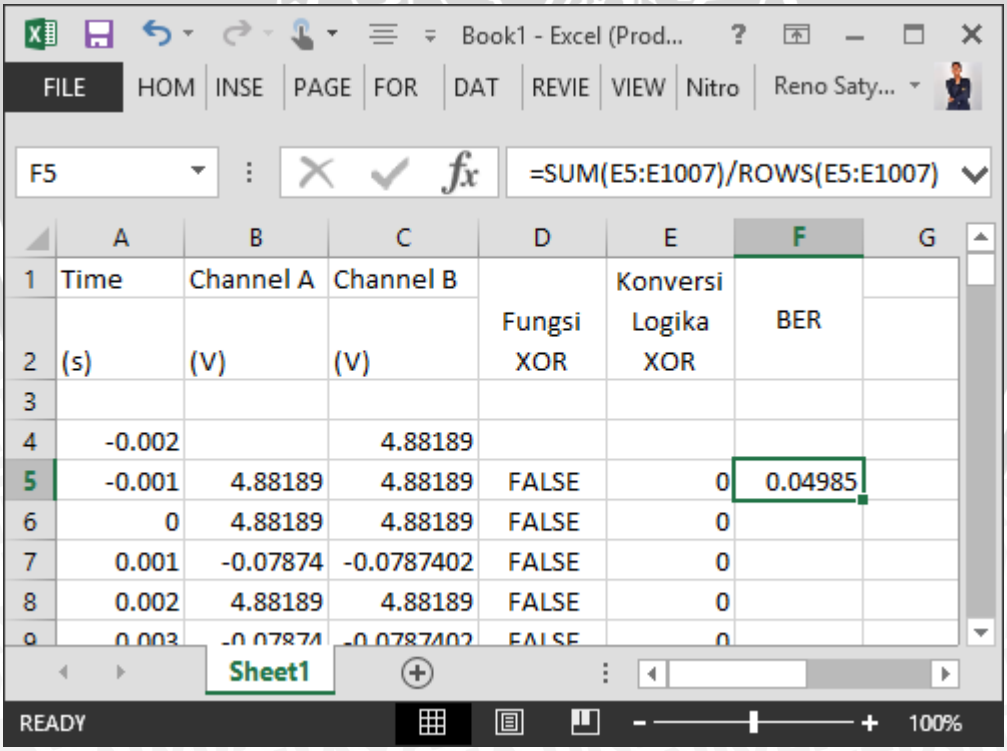
F4 =SUM(E4:E1008)/ROWS(E4:E1008)

	A	B	C	D	E	F	G
1	Time	Channel A	Channel B		Konversi		
2	(s)	(V)	(V)	Fungsi XOR	Logika XOR	BER	
3							
4	-0.002	4.88189	4.88189	FALSE	0	0.495522	
5	-0.001	4.88189	4.88189	FALSE	0		
6	0	-0.07874	4.88189	TRUE	1		
7	0.001	4.88189	-0.0787402	TRUE	1		
8	0.002	-0.07874	4.88189	TRUE	1		

Sheet1

READY 100%

(a)



Book1 - Excel (Prod...

FILE | HOM | INSE | PAGE | FOR | DAT | REVIE | VIEW | Nitro | Reno Saty...

F5 =SUM(E5:E1007)/ROWS(E5:E1007)

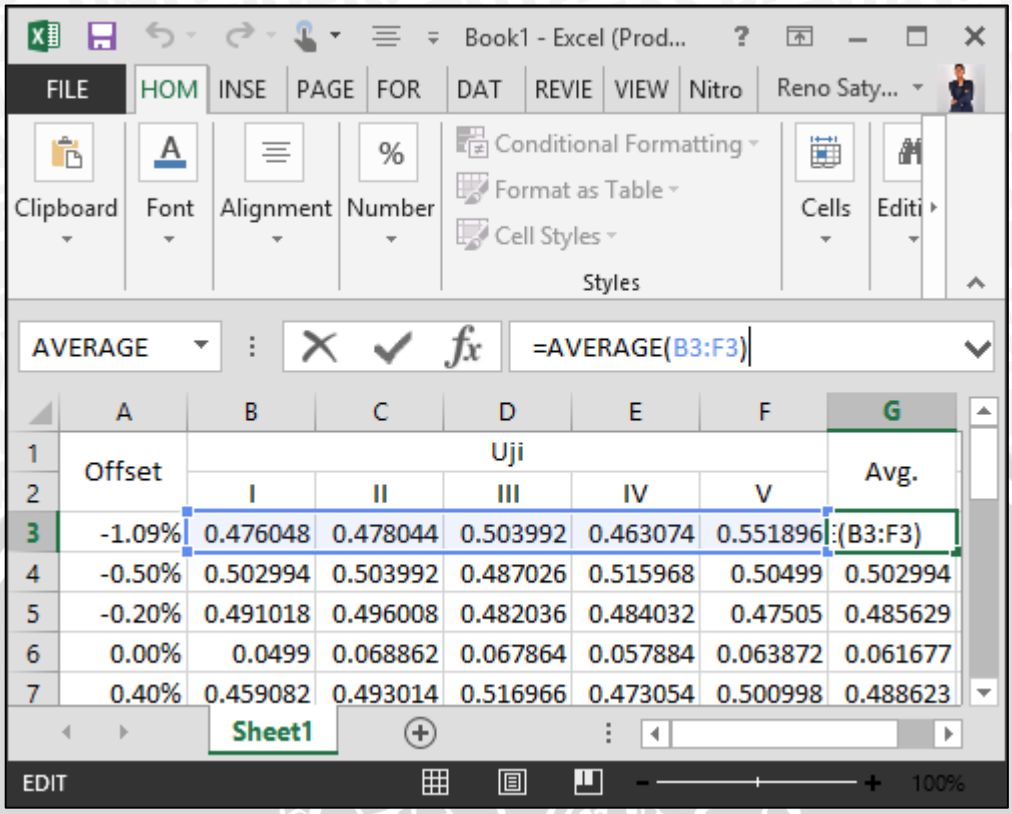
	A	B	C	D	E	F	G
1	Time	Channel A	Channel B		Konversi		
2	(s)	(V)	(V)	Fungsi XOR	Logika XOR	BER	
3							
4	-0.002		4.88189				
5	-0.001	4.88189	4.88189	FALSE	0	0.04985	
6	0	4.88189	4.88189	FALSE	0		
7	0.001	-0.07874	-0.0787402	FALSE	0		
8	0.002	4.88189	4.88189	FALSE	0		

Sheet1

READY 100%

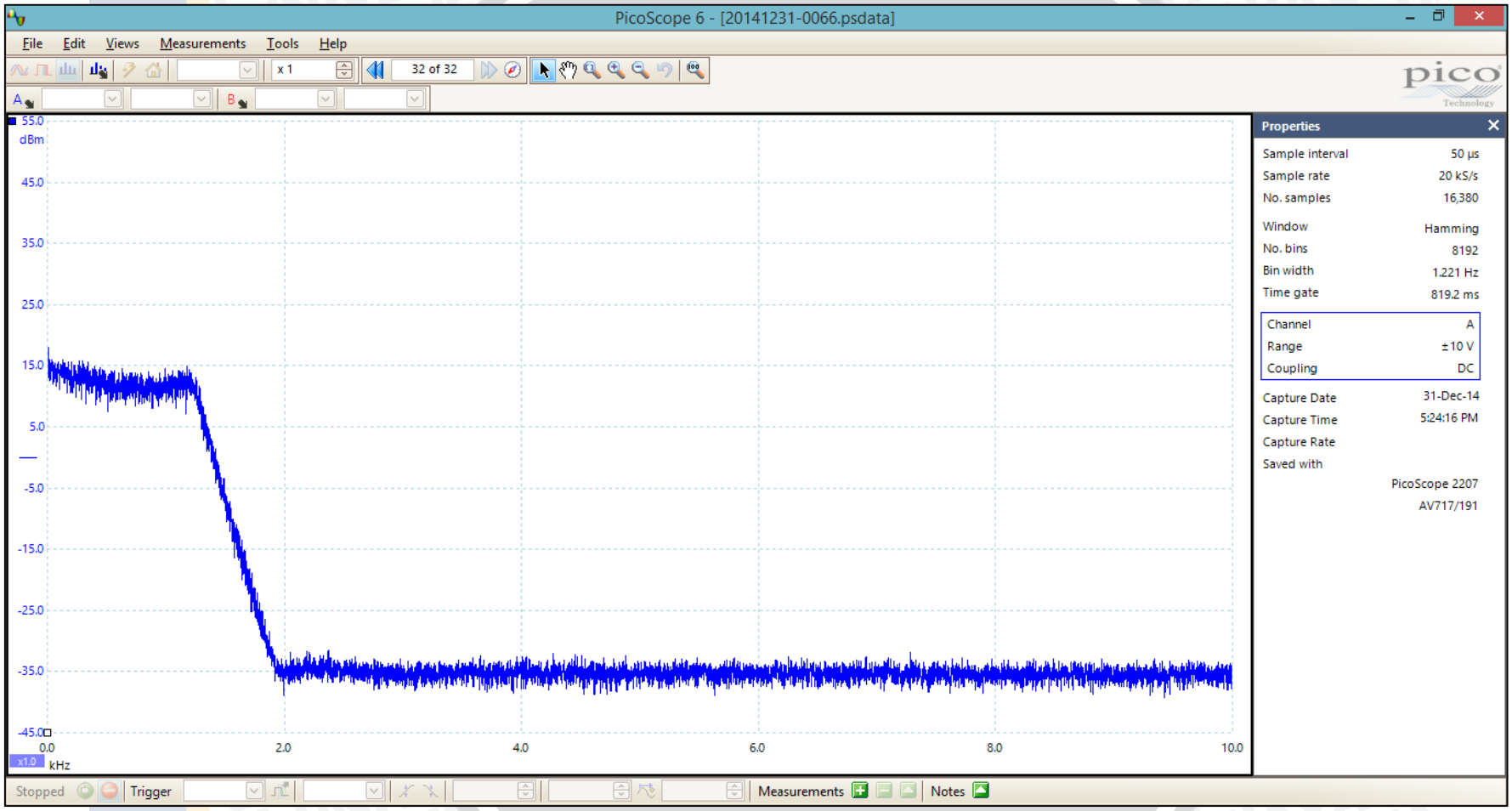
(b)

Lampiran 14 Perhitungan pada Sampel yang Berbeda dengan Frekuensi yang Sama.

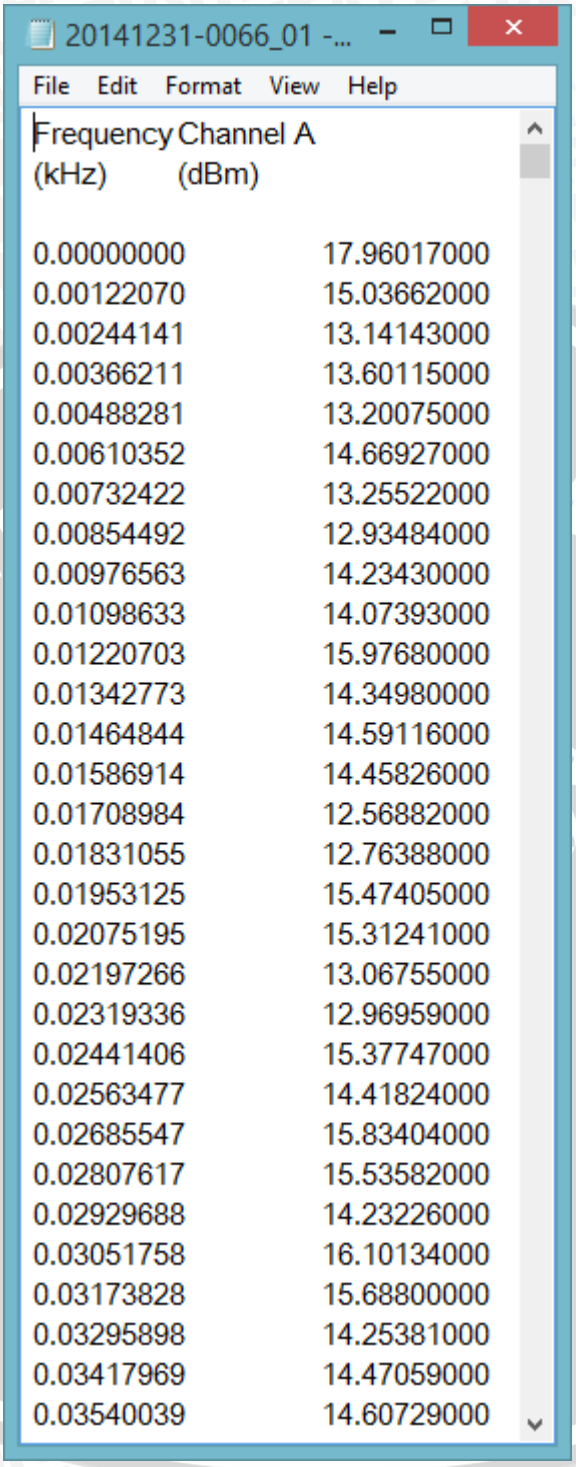


	A	B	C	D	E	F	G
1	Offset	Uji					Avg.
2		I	II	III	IV	V	
3	-1.09%	0.476048	0.478044	0.503992	0.463074	0.551896	(B3:F3)
4	-0.50%	0.502994	0.503992	0.487026	0.515968	0.50499	0.502994
5	-0.20%	0.491018	0.496008	0.482036	0.484032	0.47505	0.485629
6	0.00%	0.0499	0.068862	0.067864	0.057884	0.063872	0.061677
7	0.40%	0.459082	0.493014	0.516966	0.473054	0.500998	0.488623

Lampiran 15 Spektrum yang Diperoleh setelah Sinyal difilter dengan 32 Sampel.



Lampiran 16 Spektrum yang Diperoleh dalam Teks.



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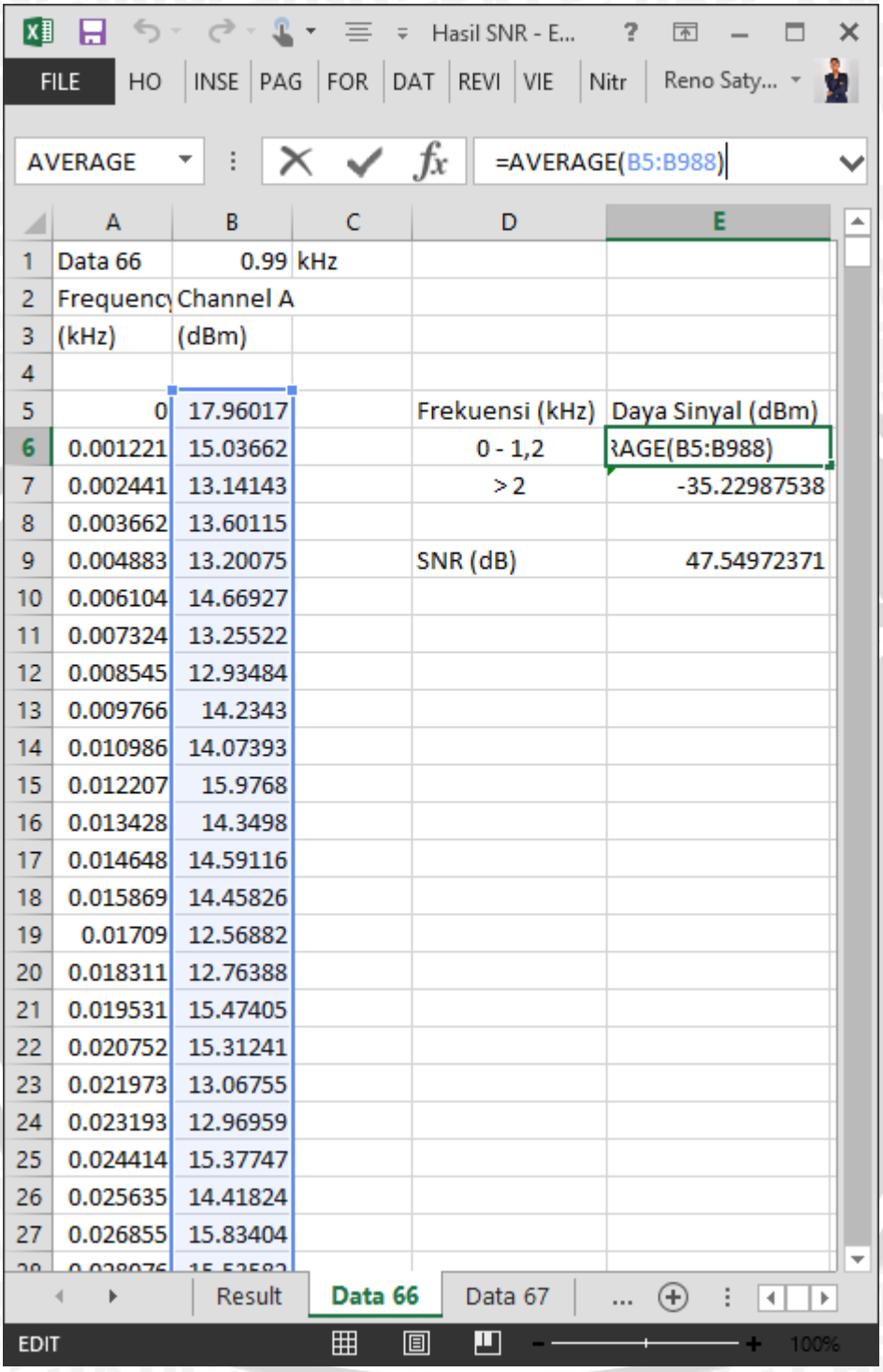
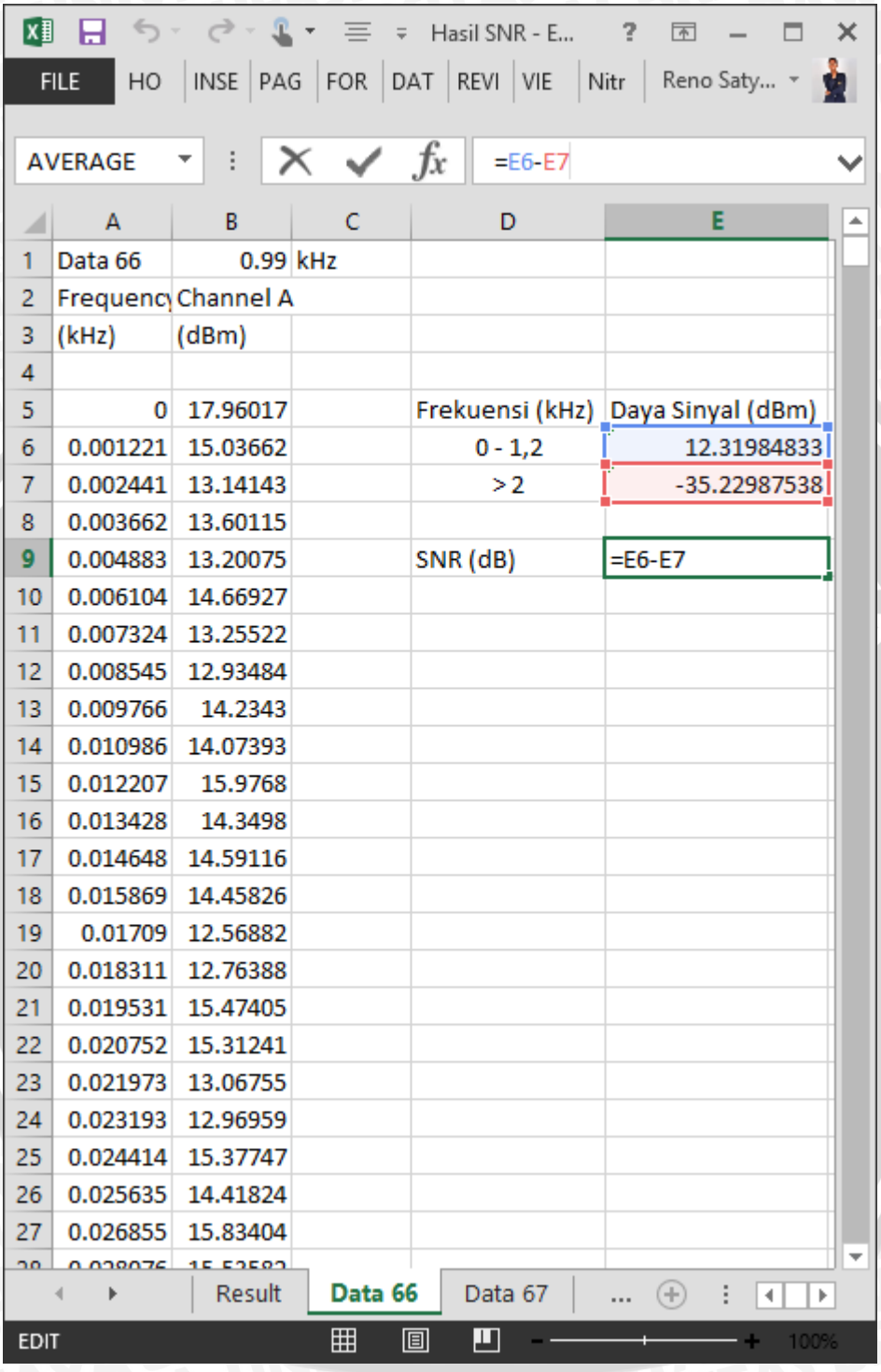
Frequency (kHz)	Channel A (dBm)
0.00000000	17.96017000
0.00122070	15.03662000
0.00244141	13.14143000
0.00366211	13.60115000
0.00488281	13.20075000
0.00610352	14.66927000
0.00732422	13.25522000
0.00854492	12.93484000
0.00976563	14.23430000
0.01098633	14.07393000
0.01220703	15.97680000
0.01342773	14.34980000
0.01464844	14.59116000
0.01586914	14.45826000
0.01708984	12.56882000
0.01831055	12.76388000
0.01953125	15.47405000
0.02075195	15.31241000
0.02197266	13.06755000
0.02319336	12.96959000
0.02441406	15.37747000
0.02563477	14.41824000
0.02685547	15.83404000
0.02807617	15.53582000
0.02929688	14.23226000
0.03051758	16.10134000
0.03173828	15.68800000
0.03295898	14.25381000
0.03417969	14.47059000
0.03540039	14.60729000

Lampiran 17 Perhitungan Daya Sinyal dan *Noise*.



	A	B	C	D	E
1	Data 66	0.99	kHz		
2	Frequency	Channel A			
3	(kHz)	(dBm)			
4					
5	0	17.96017		Frekuensi (kHz)	Daya Sinyal (dBm)
6	0.001221	15.03662		0 - 1,2	RAGE(B5:B988)
7	0.002441	13.14143		> 2	-35.22987538
8	0.003662	13.60115			
9	0.004883	13.20075		SNR (dB)	47.54972371
10	0.006104	14.66927			
11	0.007324	13.25522			
12	0.008545	12.93484			
13	0.009766	14.2343			
14	0.010986	14.07393			
15	0.012207	15.9768			
16	0.013428	14.3498			
17	0.014648	14.59116			
18	0.015869	14.45826			
19	0.01709	12.56882			
20	0.018311	12.76388			
21	0.019531	15.47405			
22	0.020752	15.31241			
23	0.021973	13.06755			
24	0.023193	12.96959			
25	0.024414	15.37747			
26	0.025635	14.41824			
27	0.026855	15.83404			

Lampiran 18 Perhitungan SNR.



Hasil SNR - E...

FILE | HO | INSE | PAG | FOR | DAT | REVI | VIE | Nitr | Reno Saty...

AVERAGE | =E6-E7

	A	B	C	D	E
1	Data 66	0.99	kHz		
2	Frequency	Channel A			
3	(kHz)	(dBm)			
4					
5	0	17.96017		Frekuensi (kHz)	Daya Sinyal (dBm)
6	0.001221	15.03662		0 - 1,2	12.31984833
7	0.002441	13.14143		> 2	-35.22987538
8	0.003662	13.60115			
9	0.004883	13.20075		SNR (dB)	=E6-E7
10	0.006104	14.66927			
11	0.007324	13.25522			
12	0.008545	12.93484			
13	0.009766	14.2343			
14	0.010986	14.07393			
15	0.012207	15.9768			
16	0.013428	14.3498			
17	0.014648	14.59116			
18	0.015869	14.45826			
19	0.01709	12.56882			
20	0.018311	12.76388			
21	0.019531	15.47405			
22	0.020752	15.31241			
23	0.021973	13.06755			
24	0.023193	12.96959			
25	0.024414	15.37747			
26	0.025635	14.41824			
27	0.026855	15.83404			

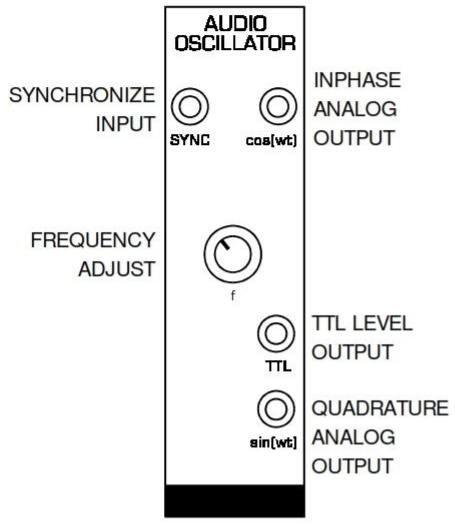
Result | Data 66 | Data 67 | ...

EDIT | 100%

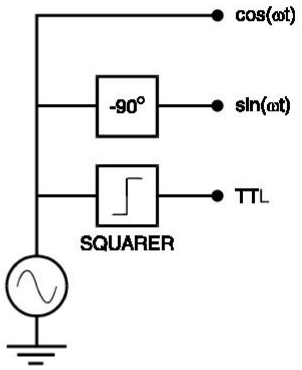
Lampiran 19 *User Manual Audio Oscillator*.

AUDIO OSCILLATOR

The AUDIO OSCILLATOR is a low distortion tuneable frequency sinewave source with a frequency range from 500Hz to 10kHz. Three outputs are provided. Two outputs are sinusoidal, with their signals in quadrature. The third output is a digital TTL level signal.



FRONT PANEL



BLOCK DIAGRAM

USE

The frequency of each of the three outputs is the same and is varied by the front panel Δ **f** control. Both the in-phase and quadrature analog output signals have fixed amplitude. Their shape is sinusoidal, having a distortion of less than 0.1%.

The AUDIO OSCILLATOR may be synchronized to an external periodic signal by connecting such a signal to the front panel **SYNC** input. A signal of about 1 volt peak is adequate for this purpose. For synchronization to be achieved, the AUDIO OSCILLATOR must be manually tuned to within a few percent of the frequency to which synchronization is desired.

BASIC SPECIFICATIONS

Frequency Range 300Hz to 10kHz
Analog Output Level 4V pk-pk
Distortion < 0.1% analog outputs only
Digital Output TTL level

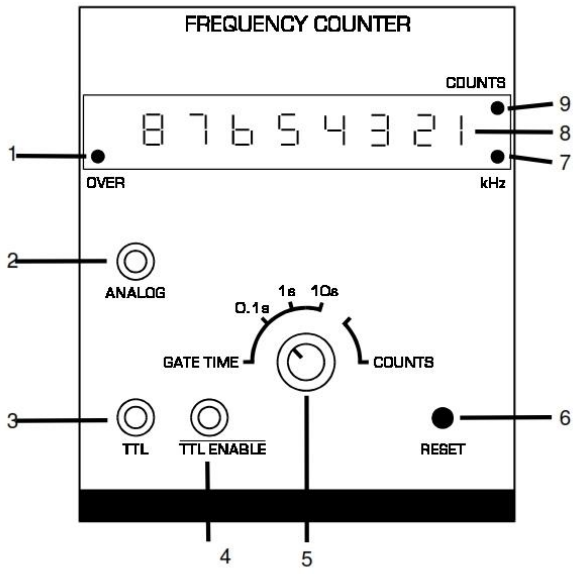
PARAMETERS TO NOTE

frequency range; relative phase of outputs; amplitude stability with frequency range; harmonic content; short term stability; synchronizing characteristic.

Lampiran 20 *User Manual Frequency Counter*.

FREQUENCY COUNTER

The TIMS counter is an 8 digit, 10MHz frequency and event counter.



BASIC SPECIFICATIONS

1 OVERflow indication LED

2 ANALOG input:

Bandwidth 40Hz to 1 MHz

Sensitivity 250mV typically, @ 100kHz

Maximum input ±12V

3 TTL Input:

Bandwidth DC to 10MHz

Input TTL level signals only

4 TTL ENABLE may be used to gate the TTL input signal.
Specifications are same as for the TTL input.

5 Mode and Range rotary switch

Frequency counter mode Gate time selection of 0.1s, 1s or 10s with reading in kHz

Event counter mode displays number of pulses counted since the last RESET

6 RESET Push Button resets the count of the Event Counter to zero

7 kHz LED is lit when counter is in FREQUENCY COUNTER mode

8 8 digit, 7 segment display of frequency or pulse counts;
maximum display 99999999

9 COUNTS LED is lit when counter is in EVENT COUNTER mode

Lampiran 21 *User Manual Integrate & Dump*.

INTEGRATE & DUMP

Two independent functional blocks are provided. The first block is a variable digital delay for TTL level clock signals, and may be used for aligning the phase of a bit clock to a data stream.

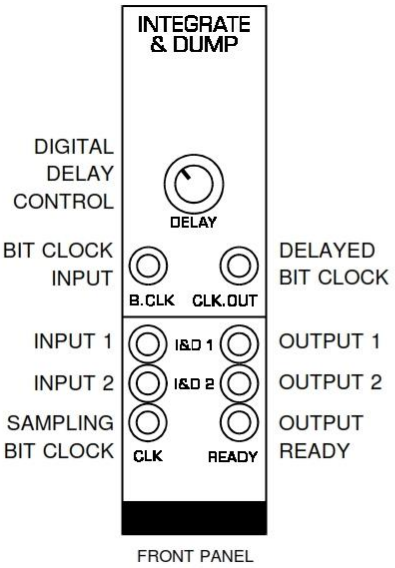
The second block includes dual channel sampling, integrate & dump and holding functions which can be switched in three combinations,

Sample & Hold;
Integrate & Dump;
Integrate & Hold.

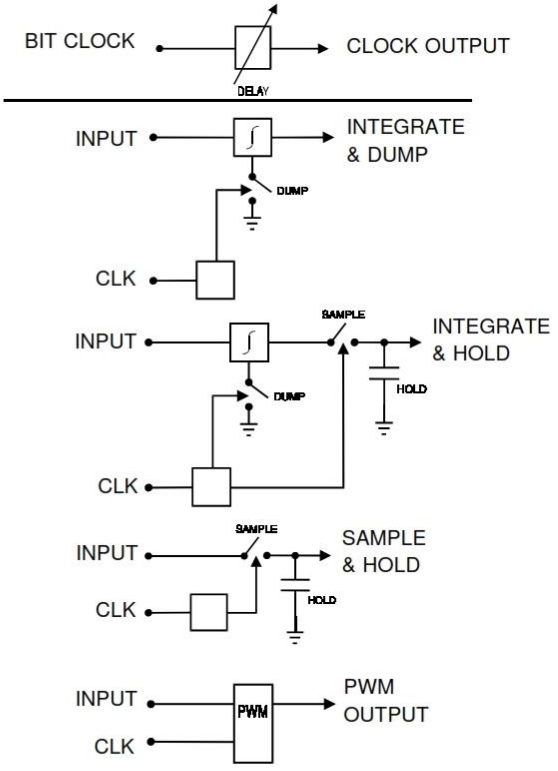
A forth, switch selectable function is only available on channel 1,

Pulse Width Modulation,

which can be used in PWM, and along with other TIMS modules, in PPM applications.



FRONT PANEL



BLOCK DIAGRAM

USE

DIGITAL DELAY

The variable digital delay accepts a standard TTL level signal at the **B.CLK** input and also outputs a standard TTL level signal at the **CLK.OUT** output.

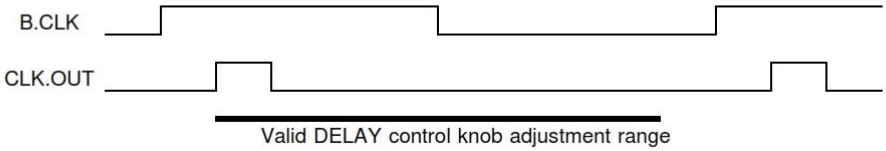
Adjusting the **DELAY** control knob provides a digital phase delay function by varying the time between the positive edge of the signal at the **B.CLK** input, with respect to the positive edge of the output signal at **CLK.OUT**. Note that the duty cycle of the input signal is not maintained during the digital delay function. The output signal at **CLK.OUT** is a fixed pulse of about 10µsec width.

Lampiran 22 *User Manual Integrate & Dump* (lanjutan)

The **DELAY** control knob will vary the digital delay time from, approximately, 10µsec to 1.5msec, over four user selectable ranges. The adjustment range is selected via the PCB mount switch, SW3. Refer to the following table for switch settings,

SW3-2 (A)	SW3-1 (B)	DELAY ranges
OFF	OFF	10µs - 100µs
OFF	ON	60µs - 500µs
ON	OFF	100µs - 1ms
ON	ON	150µs - 1.5ms

The timing diagram below illustrates the relationship between the input signal **B.CLK** and the output signal **CLK.OUT**.



Caution: always ensure that the **CLK.OUT** pulse remains within the **B.CLK** cycle, as illustrated above. Extending the **CLK.OUT** pulse into the following cycle will cause invalid operation.

SAMPLING & INTEGRATING FUNCTIONS

The sampling and integrating block provides two identical channels which operate simultaneously with a common sampling clock.

Each channel, **I&D1** and **I&D2**, takes a standard TIMS level analog input. The output signals are analog level.

The two channels require a bit clock for operation which is provided via the **CLK** input. A standard TTL level signal is required.

The **READY** output pulse is only used when *sample & hold* or *integrate & hold* functions are selected. The positive edge of the **READY** pulse occurs immediately after the signal at the **I&D1** or **I&D2** outputs has been updated and has settled.

(i) Mode select

Each channel of the sampling and integrating block includes three circuit functions: a sampler, an integrator and a hold circuit. The user can select the configuration of these circuit functions via two PCB mount, rotary switches: SW1 for channel **I&D1**, and SW2 for channel **I&D2**. The available configurations, the corresponding PCB labels and functional descriptions are given below.

Label	Function	Description
S&H1 S&H2	Sample & Hold	The input signal is sampled, held and output after the occurrence of each positive **CLK** edge.
I&H1 I&H2	Integrate & Hold	The input signal is integrated over the period of the **CLK** signal. At the occurrence of each positive **CLK** edge, the integrator value is transferred to a hold circuit, updating the value at the output. The integrator is then dumped and a new integration period commences.
I&D1 I&D2	Integrate & Dump	The input signal is integrated over the period of the **CLK** signal. During the occurrence of each **READY** pulse, the integrator is dumped and a new integration period is commenced. The integrator output is available at the channel's front panel output terminal.

(ii) Integrator time constants
The following table summarizes the components and values associated with the integrator time constant of each channel.

Channel	Integrator's R	Integrator's C	Comments
I&D1	330kohm - R7	470pF - C4	- Fixed RC
I&D2	330kohm - R26	470pF - C34	- Jumper J1 *open* : only C34 selected.
		470pF - C44	- Jumper J1 *shorted* adds C44 to C34 (jumper at the "IN" position).

IMPORTANT NOTE: The integrator both *integrates* and *inverts* the input signal.

PULSE WIDTH MODULATION FUNCTIONS
The sampling and integrating block also provides a pulse width modulation - PWM - function, on channel 1, **I&D1**. PWM mode is selected using the PCB mount rotary switch, SW1.

The analog message is presented to the **I&D1** input, with the TTL level PWM clock presented to the **CLK** input. The TTL level PWM signal is available at the **I&D1** output.

The negative or falling edge of the PWM output signal remains fixed with respect to the input PWM clock signal **CLK**: it is the *positive* or *rising edge* that varies the pulse's width.

Note that the operation of the PWM function is directly affected by *both* the amplitude of the analog message *and* the frequency of the PWM clock. Therefore these two parameters must be observed when setting up a PWM system.

(i) PWM Settings
The default amplitude and PWM clock parameters required in order to achieve a PWM signal with a 10% to 90% pulse width range are given in the table below, along with parameter limits.

PWM clock frequency at CLK input	Message amplitude at I&D1 input	Comments
1kHz	-2V to +2V	Default parameters to achieve 10% to 90% PWM
500Hz < CLK < 10kHz	+/-5V to +/-0.5V	Typical maximum and minimum parameter settings

When parameters other than the default settings are used, it is recommended that the BUFFERS module is used to scale the message amplitude for required PWM operation.

(ii) Pulse Position Modulation Function
The INTEGRATE & DUMP and the TWIN PULSE GENERATOR modules may be used together to provide a pulse position modulation function.

To set up PPM, first the INTEGRATE & DUMP module must be set up for correct PWM operation.

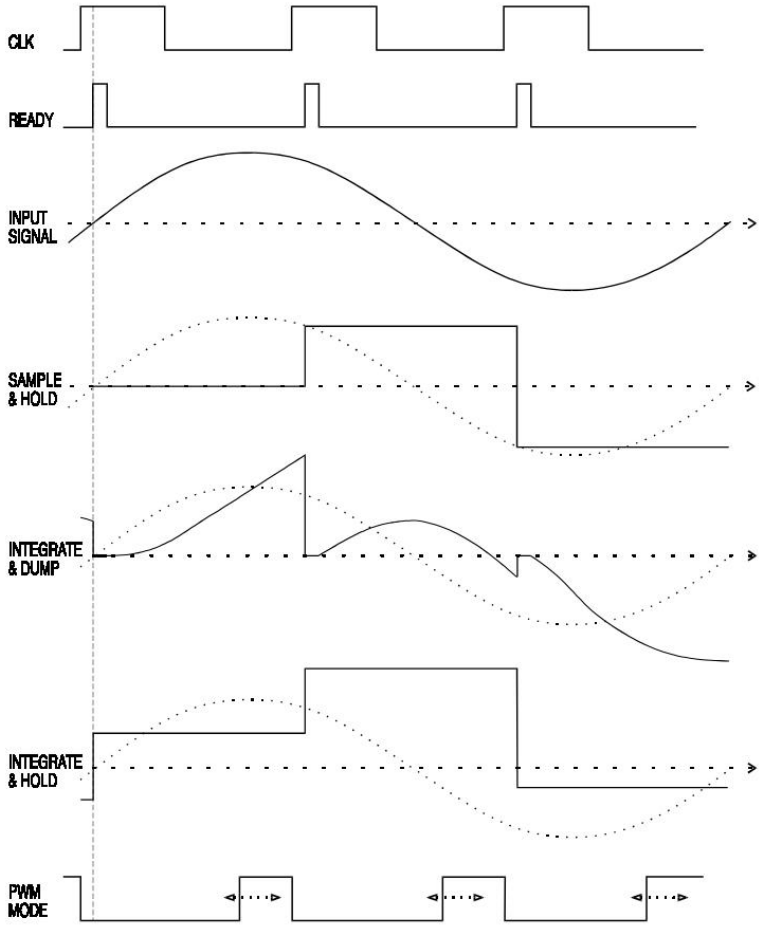
The second step is to use the PWM output signal to clock the TWIN PULSE GENERATOR module's clock input, **CLK**. Ensure that SINGLE mode is selected on the TWIN PULSE GENERATOR module's PCB mount slide switch. The TWIN PULSE GENERATOR module's outputs then both produce a pulse position modulation signal.

Take care to ensure that the TWIN PULSE GENERATOR module's pulse width is not set wider than the repetition time of the PWM pulses.

Lampiran 24 *User Manual Integrate & Dump* (lanjutan).

INTEGRATE & DUMP block function waveforms

The waveforms below illustrate the operation and timing of the sampling and integrating block's functions.



BASIC SPECIFICATIONS

DIGITAL DELAY

Input & Output TTL level, digital signals

Clock input <15kHz

Variable delay range 10µs to 1.5ms, in 4 switch selectable ranges

INTEGRATE & DUMP

Operating modes integrate & dump; integrate & hold; sample & hold; PWM.

Channels 2 channels, simultaneously operating with a common bit clock, with the exception of PWM mode, which is only available on channel 1, I&D1.

Analog inputs and outputs standard TIMS level

Clock input <500Hz to >15kHz, standard TTL level

Integrator integration commences on the negative edge of the READY signal. When hold is selected, the integrator output is sampled on the positive edge of the clock signal. Dumping commences on the positive edge of the READY pulse. The output of the integrator is inverting.

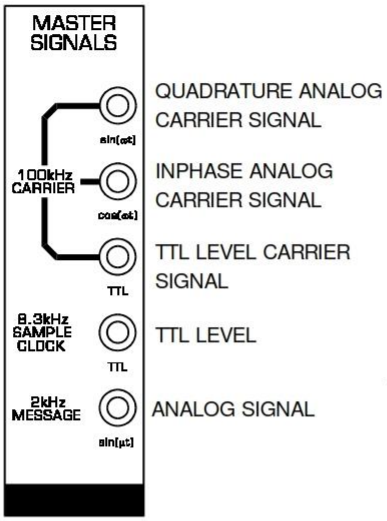
Sampler the sampling of the input signal commences on the positive edge of the clock signal and is completed on the positive edge of the READY pulse.

Ready TTL level pulse, <10µs width. Occurs after the hold circuit's output has settled.

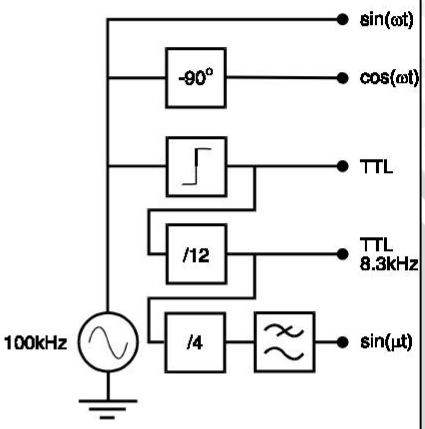
Lampiran 25 *User Manual Master Signals.*

MASTER SIGNALS

Five synchronized analog and digital signals are available, ranging from 2kHz to 100kHz. The function and frequency of each signal is indicated on the front panel.



FRONT PANEL



BLOCK DIAGRAM

USE

Signals are labelled as follows:

CARRIER signals are 100kHz, which for modelling purposes is sufficiently far from the audio channel bandwidth of 3kHz.

The **SAMPLE CLOCK** of 8.3kHz, which may be used to sample bandwidth-limited (3kHz) audio message signals.

MESSAGE provides an audio frequency signal which is synchronized to a sub-multiple of the carrier to enable 'text-book' like displays of simple modulation schemes to be achieved.

The five signals are derived from a master crystal oscillator resulting in low frequency drift. Their frequencies are fixed internally. The output levels are also fixed. To vary the amplitude, the signals may be applied to the neighboring buffers.

The analog signals are sinusoidal in shape, having a distortion of less than 0.1%.
Digital signals are all standard TTL level, with rise times of better than 80nsec.

Lampiran 26 *User Manual Master Signals* (lanjutan).

BASIC SPECIFICATIONS

Output Frequencies 100kHz, carrier
8.333kHz, sample clock
2.083kHz, audio (carrier sub-multiple)

Output Levels 4V pk-pk, analog
TTL level, digital

Distortion < 0.1%, analog outputs only

PARAMETERS TO NOTE

short term frequency stability; relative phase of quadrature outputs; harmonic content.

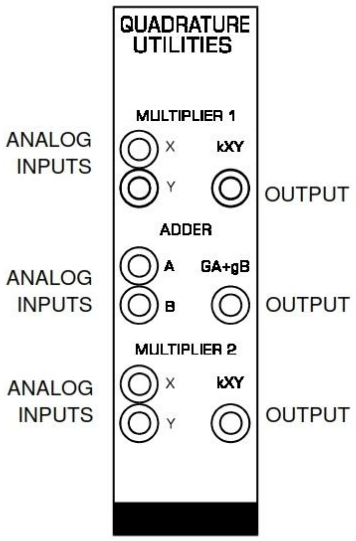
Lampiran 27 *User Manual Quadrature Utilities.*

QUADRATURE UTILITIES

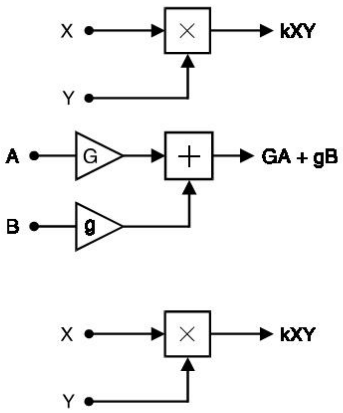
Three independent functions are provided: two independent multipliers and an independent adder.

Each MULTIPLIER allows two analog signals **X(t)** and **Y(t)** to be multiplier together. The resulting product is scaled by a factor of approximately 1/2.

The ADDER allows two input signals **A(t)** and **B(t)** to be added together, in adjustable proportions **G** and **g**.



FRONT PANEL



BLOCK DIAGRAMS

USE

(i) MULTIPLIER 1 and MULTIPLIER 2
Each multiplier has two inputs. The inputs and outputs are DC coupled. The "k" factor (a scaling parameter associated with "four quadrant" multipliers) is approximately one half. It is defined with respect to the OUTPUT of the multiplier and may be measured experimentally.

(ii) ADDER
The adder input gains G and g can be adjusted via pcb mounted trimmers RV1 and RV3, respectively. Note that these two trimmers have knobs to allow for finger adjustment.

RV1 varies **G** and **RV3** varies **g**

BASIC SPECIFICATIONS

MULTIPLIER 1 and MULTIPLIER 2
Inputs & Outputs DC coupled
Bandwidth approx. 1MHz
Characteristic k.X(t).Y(t); **k** is approx. 1/2

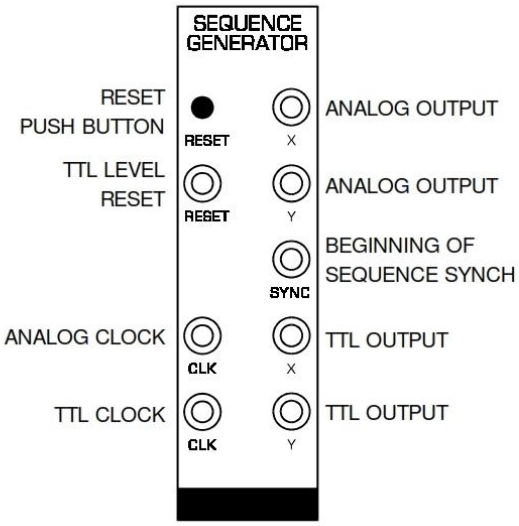
ADDER
Gain range 0 < G & g < 1.5
Bandwidth approx. 500kHz

Lampiran 28 *User Manual Sequence Generator*.

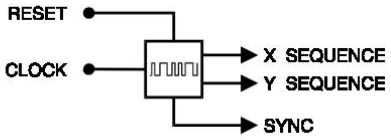
SEQUENCE GENERATOR

(PSEUDORANDOM SEQUENCE GENERATOR)

Using a common external clock signal, the sequence generator outputs two independent pseudorandom sequences **X** and **Y**. A **SYNC** output is provided which is coincident with the start of the sequences. The sequences may be stopped and restarted at any time via front panel controls. Sequences **X** and **Y** are available as either standard TTL or analog level output.



FRONT PANEL



BLOCK DIAGRAM

USE

An external clock signal must be provided to operate the SEQUENCE GENERATOR. This may be sinusoidal or TTL: separate input sockets are used.

The sequences may be stopped at any time by either depressing the **RESET button** or applying a TTL HI signal to the **RESET input**. To restart the sequences from the beginning, release the **RESET button** or apply a TTL LO to the **RESET input.**

The length of the sequences may be selected by a PCB mounted dip switch. Four independent sequence pairs are available from lengths of 2^5 to 2^{11}.

The sequences are selected as follows:

DIP SWITCH CODE		n	SEQUENCE LENGTH 2^n
msb 0	0	5	32
0	1	8	256
1	0	8	256
1	1	11	2048

Lampiran 29 *User Manual Sequence Generator* (lanjutan).

BASIC SPECIFICATIONS

Input Clock Range TTL 1Hz to 1MHz
Analog < 500Hz to > 10kHz
Number of Sequences 4 pairs
Sequence Lengths 2^5, 2^8, 2^8, 2^{11}
Sync indicates start of sequence

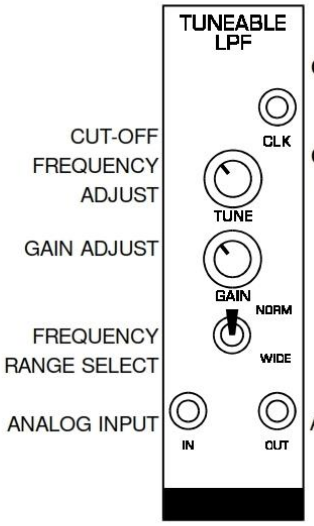
PARAMETERS TO NOTE

sequence distribution; noise generation using pseudorandom sequences.

Lampiran 30 *User Manual Tuneable* LPF.

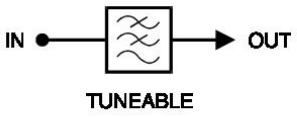
TUNEABLE LPF

The cutoff frequency of this LOWPASS FILTER can be varied using the **TUNE** control. Two frequency ranges, **WIDE** and **NORMAL**, can be selected by a front panel switch. The **GAIN** control allows signal amplitudes to be varied if required.



FRONT PANEL

CLK for TLPF modules V1 to V3:
CLK/880 = f_{-3dB}; NORMAL
CLK/360 = f_{-3dB}; WIDE
CLK for TLPF modules V4:
CLK/100 = f_{-3dB}; NORMAL & WIDE



BLOCK DIAGRAM

USE

This lowpass filter has an elliptic filter characteristic. The stopband attenuation is typically 50dB and passband ripple is approximately 0.5dB.

The **GAIN** control is used to vary the amplitude of the output signal. Care should be taken to avoid overloading/saturation. Two frequency ranges are provided. **NORM**AL range provides more precise control over the lower audio band, used for telecommunications message channels. The **WIDE** range expands the filter's range to above 10kHz. The **CLK** output provides an indication of the filter's cutoff frequency.

BASIC SPECIFICATIONS for TLPF modules V1 to V3

Filter Ranges 900 Hz < NORMAL < 5 kHz and
2.0 kHz < WIDE < 12 kHz, continuously variable over each range.
Filter Order 7th order, Elliptic
Stopband Attenuation > 50dB and **Passband Ripple** < 0.5dB

BASIC SPECIFICATIONS for TLPF modules V4

Filter Ranges 200 Hz < NORMAL < 5 kHz and
200 Hz < WIDE < 12 kHz, continuously variable over each range.
Filter Order 5th order, Elliptic
Stopband Attenuation > 50dB and **Passband Ripple** < 0.5dB
Maximum Input Voltage + 5V to -5V (TTL-level input signal is acceptable)

PARAMETERS TO NOTE

corner point; phase shift; gain range; passband ripple; out of band attenuation.

Lampiran 31 *User Manual Utilities Module*.

UTILITIES MODULE

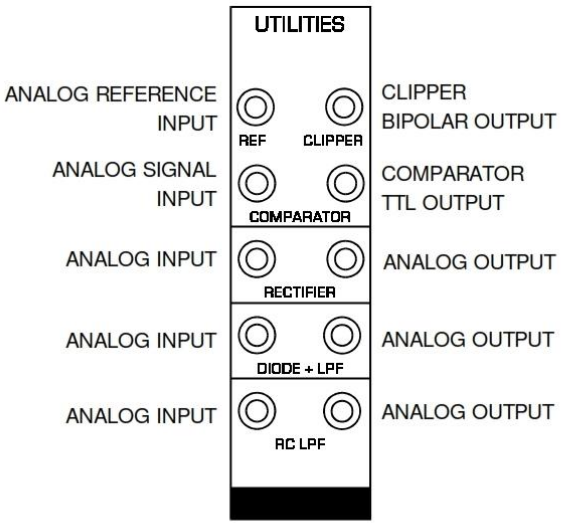
The Utilities Module houses 4 independent functional blocks:

(i) A signal COMPARATOR with TTL output and CLIPPER with bipolar output, for squaring analog waveforms. The COMPARATOR's threshold level may be set as required by applying a DC voltage to the REF input. The CLIPPER's gain may be set by adjusting DIP switches **SW1** and **SW2**.

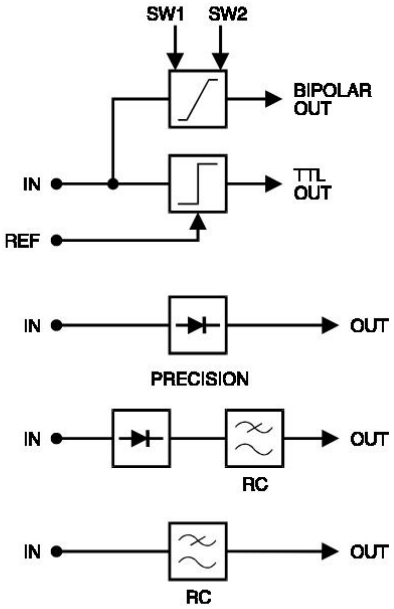
(ii) Precision halfwave RECTIFIER.

(iii) Simple diode and single pole, audio range, RC Lowpass Filter.

(iv) Single pole, audio range, RC Lowpass Filter.



FRONT PANEL



BLOCK DIAGRAM

USE

COMPARATOR

The COMPARATOR will square any analog signal and provide a standard TTL level output. The switching threshold level is determined by the voltage level applied to the **REF** input.

NOTE: *For correct COMPARATOR operation, the **REF** input must never be left unconnected.* The **REF** input may be connected to GROUND, VARIABLE DC or any other signal source.

CLIPPER

The CLIPPER will amplify any analog TIMS level signal and then clip the amplitude of the amplified signal, to a fixed level of approximately ± 1.8V. The clipping action is performed by standard small signal diodes.

NOTE: *The **REF** input is NOT used by the CLIPPER.*

Lampiran 32 *User Manual Utilities Module* (lanjutan).

Adjusting the gain of the CLIPPER, determines whether the clipping action is "*SOFT*", "*MEDIUM*" or "*HARD*". The following table, UTIL-1, relates DIP switch settings to CLIPPER gains and clipping action,

CLIPPING ACTION	GAIN (approx)	DIP SWITCH SETTINGS	
		SW1 (both a & b)	**SW2** (both a & b)
SOFT	x0.8	ON - ON	OFF - OFF
MEDIUM	x8	OFF - OFF	OFF - OFF
HARD	x40	OFF - OFF	ON - ON
-	not applicable	ON - ON	ON - ON

Table UTIL-1: CLIPPER gain settings

DIP switches SW1 and SW2 will be found in the middle of the UTILITIES module's circuit board.
NOTE: *Both halves (bits) of each switch must be in the SAME position at all times.*

BASIC SPECIFICATIONS

COMPARATOR
Operating Range > 500kHz
TTL Output Risetime 100nsec (typ)

CLIPPER
Operating Range > 500kHz
Output Level 1.8Vpk (typ)
Adjustable Gains 3 steps; x0.8, x8 and x40 (approx)

RECTIFIER
Bandwidth DC to 500kHz (approx)

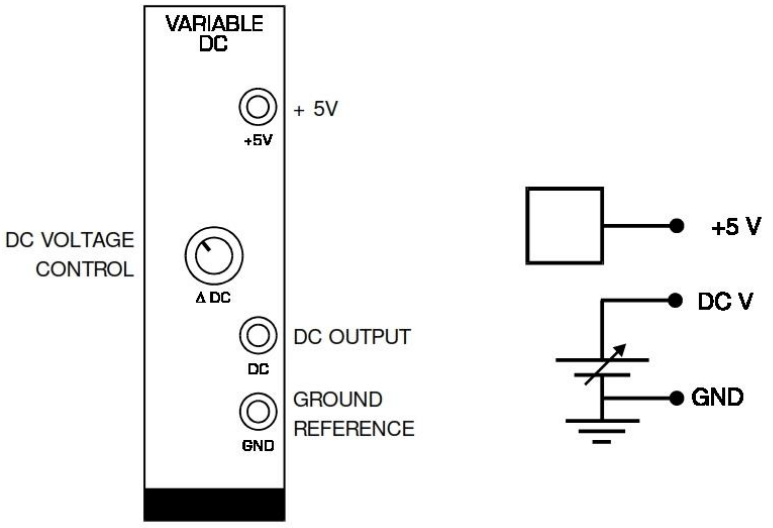
DIODE & LPF
LPF -3dB 2.8kHz (approx)

RC LPF
LPF -3dB 2.8kHz (approx)

Lampiran 33 *User Manual Variable* DC.

VARIABLE DC

The VARIABLE DC module is a stable, bipolar DC source.



FRONT PANEL BLOCK DIAGRAM

USE

The DC voltage output varies from about -2.5V when the control is fully counter clockwise through zero to + 2.5V when control is turned fully clockwise. If greater resolution or wider range is required, then one of the BUFFER AMPLIFIERS can be used in conjunction with the VARIABLE DC module.

BASIC SPECIFICATIONS

Voltage Range ± 2.5V DC
Short-term Stability < 2mV/hr
Resolution approx 20mV
Output Current < 5mA