LAMPIRAN

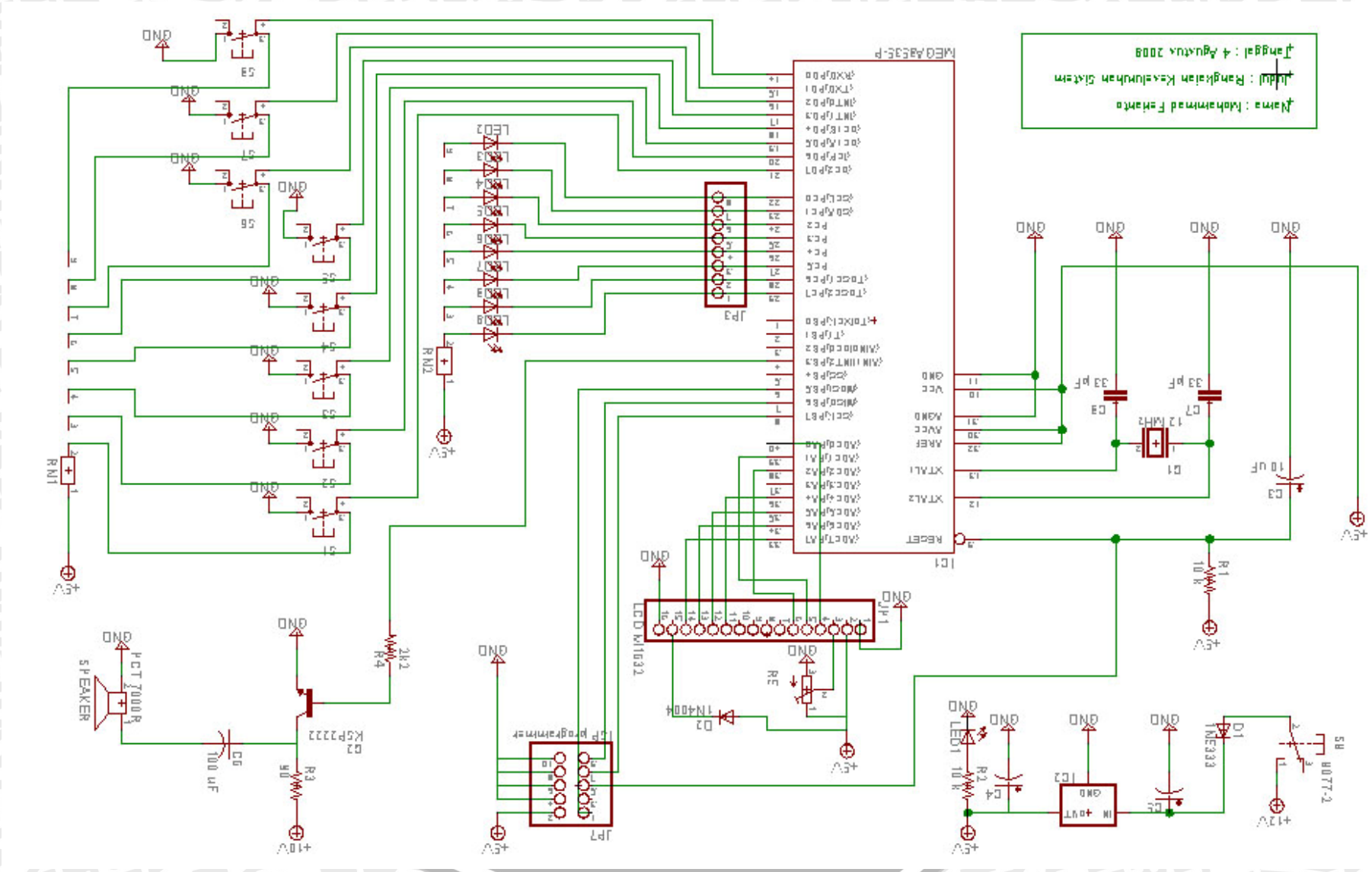
LAMPIRAN 1

Foto Alat
dan
Skema Rangkaian

Foto Alat Keseluruhan

Box Alat

Piezoelectric Speaker



LAMPIRAN 2

- Listing Program -

```
/*****************************************************
This program was produced by the
CodeWizardAVR V1.24.8d Professional
Automatic Program Generator
© Copyright 1998-2006 Pavel Haiduc, HP InfoTech s.r.l.
http://www.hpinfotech.com

Chip type           : ATmega8535
Program type        : Application
Clock frequency     : 12.000000 MHz
Memory model        : Small
External SRAM size  : 0
Data Stack size     : 128
*****************************************************/

#include <mega8535.h>
#include <delay.h>
// Alphanumeric LCD Module functions
#asm
   .equ __lcd_port=0x1b ; PORTA
#endasm
#include <lcd.h>

#define tombol_1_on             PIND.0==0
#define tombol_2_on             PIND.1==0
#define tombol_3_on             PIND.2==0
#define tombol_4_on             PIND.3==0
#define tombol_5_on             PIND.4==0
#define tombol_6_on             PIND.5==0
#define tombol_7_on             PIND.6==0
#define tombol_8_on             PIND.7==0
#define f5_kHz                  OCR0=149
#define f16koma2_kHz            OCR0=45
#define f20_kHz                 OCR0=37
#define f25_kHz                 OCR0=29
#define f30_kHz                 OCR0=24
#define f35_kHz                 OCR0=20
#define f40_kHz                 OCR0=18
#define f45_kHz                 OCR0=16
#define LED1_on         PORTC=0b11111110
#define LED2_on         PORTC=0b11111101
#define LED3_on         PORTC=0b11111011
#define LED4_on         PORTC=0b11110111
#define LED5_on         PORTC=0b11101111
#define LED6_on         PORTC=0b11011111
#define LED7_on         PORTC=0b10111111
#define LED8_on         PORTC=0b01111111

void main(void)
{

PORTA=0x00;
DDRA=0x00;

PORTB=0x00;         //ga di pull-up
DDRB=0x08;          // OC0 di port B3. B3=1 (sbg output)


PORTC=0xFF;          //pull-up
DDRC=0xFF;          //portc output

PORTD=0xFF;         //pull-up
DDRD=0x00;          //input

// Timer/Counter 0 initialization
// Clock source: System Clock
// Clock value: 1500.000 kHz
```

```
// Mode: CTC top=OCR0
// OC0 output: Toggle on compare match
TCCR0=0x1A;
TCNT0=0x00;
OCR0=0x00;

lcd_init(16);

lcd_gotoxy(0,0); lcd_putsf("Pengendali Tikus");
lcd_gotoxy(2,1); lcd_putsf("dg Ultrasonik");

while (1)
 {
 int A;
 if (tombol_1_on){f5_kHz; LED1_on; lcd_clear(); A=1;} else
 if (tombol_2_on){f16koma2_kHz; lcd_clear();LED2_on; A=2;} else
 if (tombol_3_on){f20_kHz; lcd_clear();LED3_on; A=3;} else
 if (tombol_4_on){f25_kHz; lcd_clear();LED4_on; A=4;} else
 if (tombol_5_on){f30_kHz; lcd_clear();LED5_on; A=5;} else
 if (tombol_6_on){f35_kHz; lcd_clear();LED6_on; A=6;} else
 if (tombol_7_on){f40_kHz; lcd_clear();LED7_on; A=7;} else
 if (tombol_8_on){f45_kHz; lcd_clear();LED8_on; A=8;}
 delay_ms(120);


 if (A==1)
    {//lcd_clear();
    lcd_gotoxy(0,0);lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(6,1);lcd_putsf("5 kHz");} else
 if (A==2)
    {//lcd_clear();
    lcd_gotoxy(0,0);lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1);lcd_putsf("16,2 kHz");} else
 if (A==3)
    {//lcd_clear();
    lcd_gotoxy(0,0);lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1);lcd_putsf("20 kHz");} else
 if (A==4)
    {//lcd_clear();
    lcd_gotoxy(0,0);lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1);lcd_putsf("25 kHz");} else
 if (A==5)
    {//lcd_clear();
    lcd_gotoxy(0,0); lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1); lcd_putsf("30 kHz");} else
 if (A==6)
    {//lcd_clear();
    lcd_gotoxy(0,0); lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1); lcd_putsf("35 kHz");} else
 if (A==7)
    {//lcd_clear();
    lcd_gotoxy(0,0); lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1); lcd_putsf("40 kHz");} else
 if (A==8)
    {//lcd_clear();
    lcd_gotoxy(0,0); lcd_putsf("Frekuensi aktif:");
    lcd_gotoxy(5,1); lcd_putsf("45 kHz");}
 };
}
```

LAMPIRAN 3

- Datasheet -

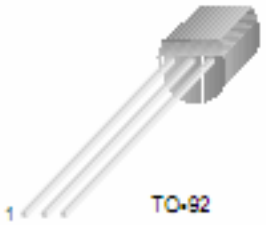
Transistor KSP2222

FAIRCHILD
SEMICONDUCTOR™

KSP2222

General Purpose Transistor

- Collector-Emitter Voltage: V_{CEO}= 30V
- Collector Dissipation: P_C (max)=625mW



TO-92

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	60	V
V_{CEO}	Collector-Emitter Voltage	30	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	600	mA
P_C	Collector Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=10μA, I_E=0	60			V
BV_{CEO}	Collector Emitter Breakdown Voltage	I_C=10mA, I_B=0	30			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=10μA, I_C=0	5			V
I_{CBO}	Collector Cut-off Current	V_{CB}=50V, I_E=0			10	nA
h_{FE}	DC Current Gain	V_{CE}=10V, I_C=0.1mA V_{CE}=10V, I_C=1mA V_{CE}=10V, I_C=10mA V_{CE}=10V, *I_C=150mA V_{CE}=10V, *I_C=500mA	35 50 75 100 30		 300 	
V_{CE} (sat)	* Collector-Emitter Saturation Voltage	I_C=150mA, I_B=15mA I_C=500mA, I_B=50mA			0.4 1.6	V V
V_{BE} (sat)	* Base Emitter Saturation Voltage	I_C=150mA, I_B=15mA I_C=500mA, I_B=50mA			1.3 2.6	V V
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz			8	pF
f_T	Current Gain Bandwidth Product	V_{CE}=20V, I_C=20mA f=100MHz	250			MHz
t_{ON}	Turn On Time	V_{CC}=30V, $V_{BE(off)}$=0.5V I_C=150mA, I_{B1}=15mA			35	ns
t_{OFF}	Turn Off Time	V_{CC}=30V, I_C=150mA I_{B1}=I_{B2}=15mA			285	ns

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Typical Characteristics

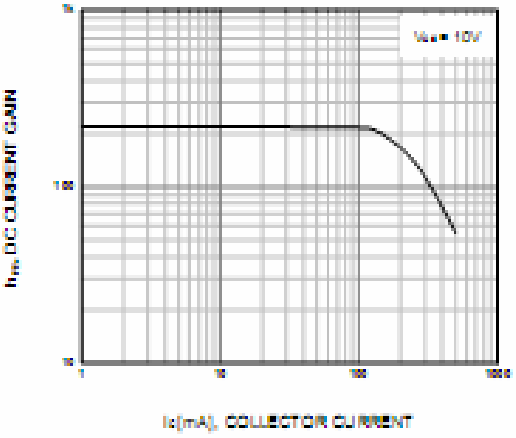


Figure 1. DC current Gain

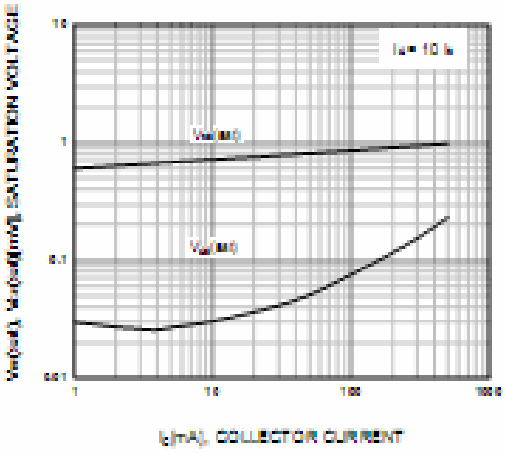


Figure 2. Collector-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

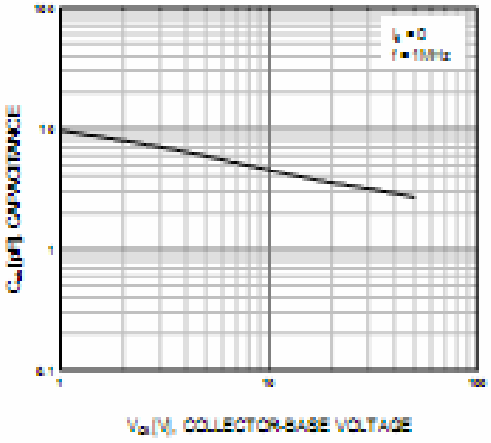


Figure 3. Collector Output Capacitance

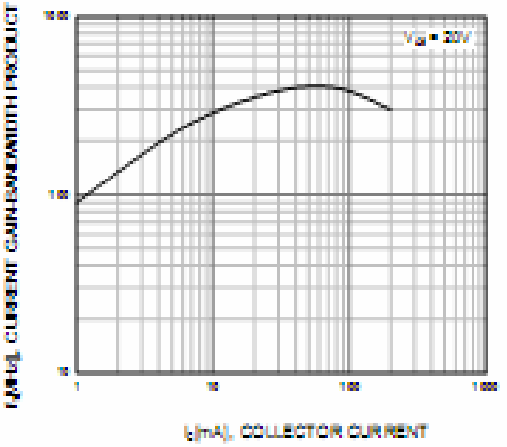
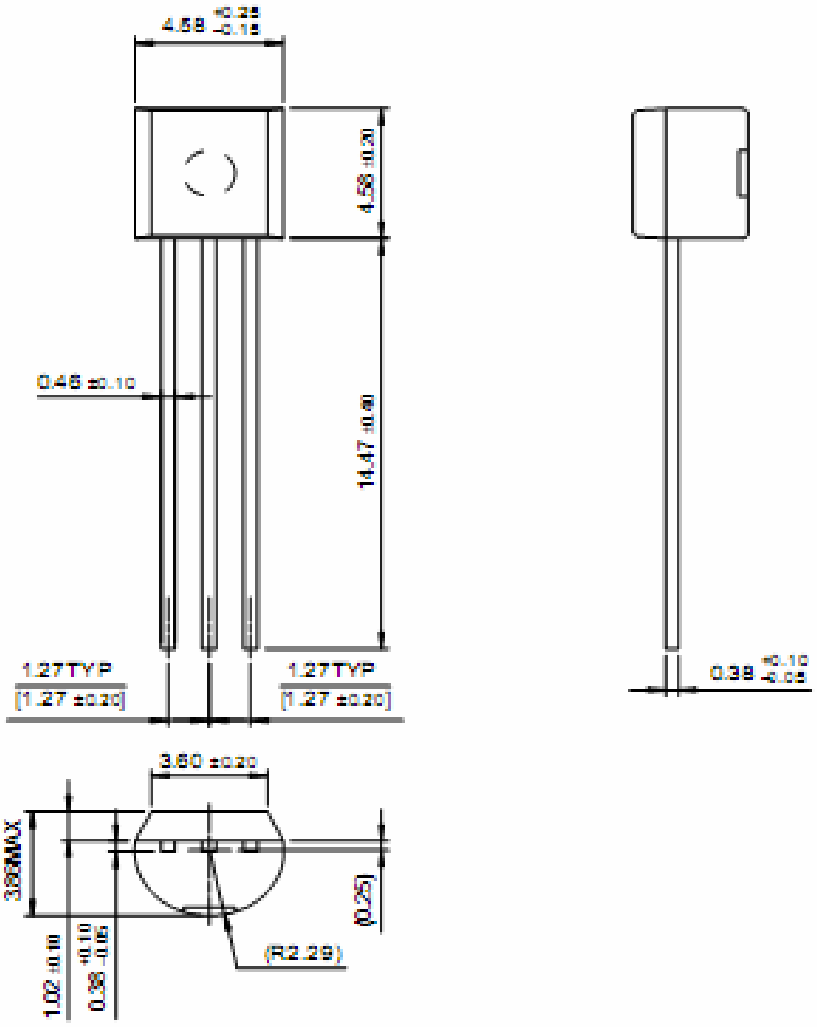


Figure 4. Current Gain Bandwidth Product

Package Demensions

TO-92



Dimensions in Mil

LCD M1632 (LMB162A)

1. BASIC SPECIFICATIONS

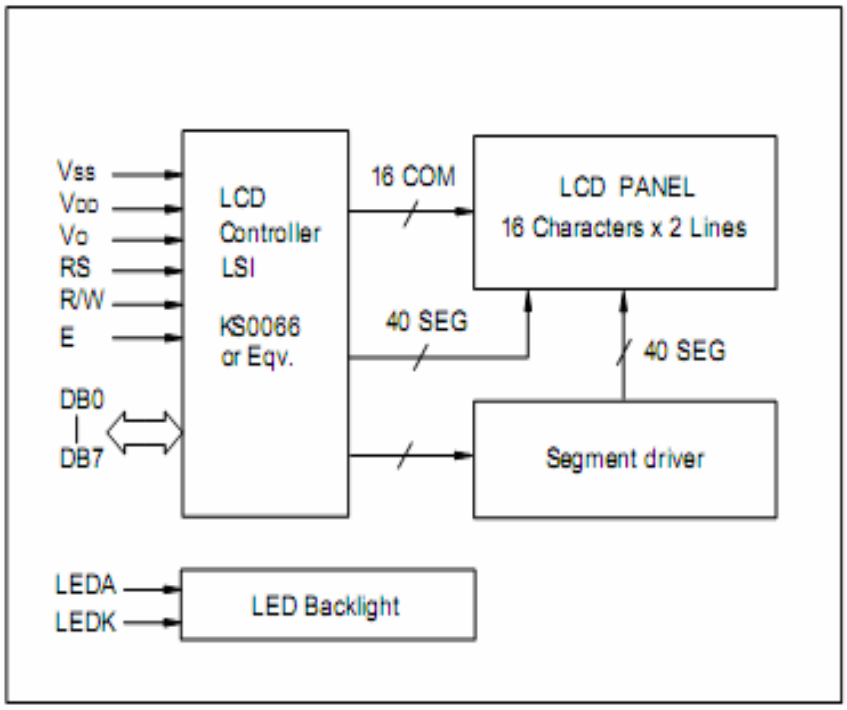
1.1 Display Specifications

LCD Mode	:	STN—Positive—Transflective
Display Color	:	Dark Blue
Background Color	:	Yellow-Green
Driving Duty	:	1/16 Duty
Viewing Direction	:	6:00
Backlight	:	LED

1.2 Mechanical Specifications

Outline Dimension	:	80.0(W) X 36.0(H) X 14.0(T)	mm
Viewing Area	:	64.6(W) X 16.0(H)	mm
Number of Characters	:	16 Characters X 2 Lines	
Character Size	:	2.95 X 5.55	mm
Dot Size	:	0.55 X 0.65	mm
Weight	:		

1.3 Block Diagram



1.4 Terminal Functions

Pin No.	Symbol	Level	Function
1	VSS	-	Ground
2	VDD	-	Power Supply for Logic (+5V)
3	VO	-	Power Supply for LCD
4	RS	H/L	Register Selection H: Display Data L: Instruction Code
5	R/W	H/L	Read/Write Selection H: Read Operation L: Write Operation
6	E	H, H→L	Enable Signal. Read data when E is "H", write data at the falling edge of E.
7	DB0	H/L	In 8-bit mode, used as low order bi-directional data bus. In 4-bit mode, open these terminals.
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	In 8-bit mode, used as high order bi-directional data bus. In 4-bit mode, used as both high and low order data bus.
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	LEDA	--	LED Power Supply (+5V)
16	LEDK	--	LED Power Supply (0v)

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage(Logic)	VDD-VSS	-0.3	7.0	V
Supply Voltage(LCD)	VDD-VO	-0.3	13.0	V
Input Voltage	VI	-0.3	VDD+0.3	V
Operating Temp.	Topr	-20	70	℃
Storage Temp.	Tstg	-30	80	℃

3. ELECTRICAL CHARACTERISTICS

3.1 DC Characteristics (VDD=5.0V±10%, Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	UNIT
Supply Voltage (Logic)	VDD		4.5	5.0	5.5	V
Supply Voltage (LCD Drive)	VDD-VO		--	5.0	--	V
Input High Voltage	VIH		2.2	--	VDD	V
Input Low Voltage	VIL		-0.3	--	0.6	V
Output High Voltage	VOH	IOH=-0.2mA	2.4	--	VDD	V
Output Low Voltage	VOL	IOL=1.2mA	0	--	0.4	V
Supply Current (Logic)	IDD	VDD=5.0V	--	1.5	3.0	mA

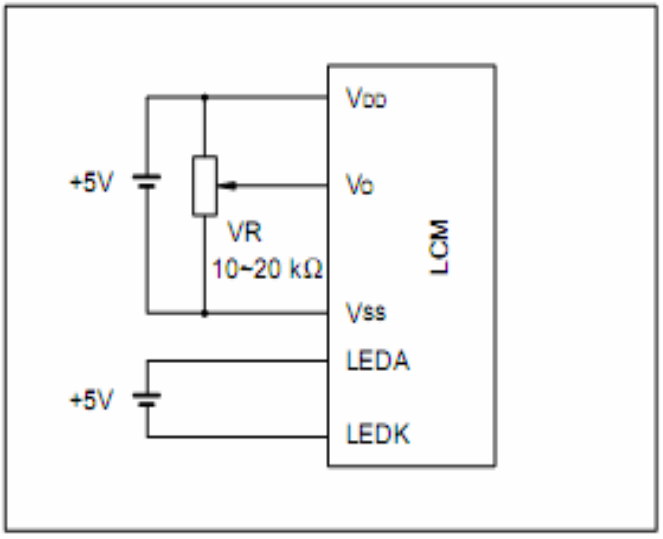
3.2 Interface Timing Chart (VDD=5.0V±10%, Ta=25℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode Refer to fig.1	E Cycle Time	t_C	500	--	--	ns
	E Rise/Fall Time	t_R, t_F	--	--	20	
	E Pulse Width (High,Low)	t_W	230	--	--	
	R/W and RS Setup Time	t_{SU1}	40	--	--	
	R/W and RS Hold Time	t_{H1}	10	--	--	
	Data Setup Time	t_{SU2}	80	--	--	
	Data Hold Time	t_{H2}	10	--	--	
Read Mode Refer to fig.2	E Cycle Time	t_C	500	--	--	ns
	E Rise/Fall Time	t_R, t_F	--	--	20	
	E Pulse Width (High,Low)	t_W	230	--		
	R/W and RS Setup Time	t_{SU}	40	--		
	R/W and RS Hold Time	t_H	10	--		
	Data Output Delay Time	t_D	--	--	120	
	Data Hold Time	t_{DH}	5	--	--	

3.3 LED Backlight Characteristics (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	UNIT
Forward Voltage	Vf		3.9	4.1	4.3	V
Forward Current	If	Vf=4.1V	--	110	--	mA
Peak Wave Length	λp	If=110mA	--	568	--	nm
Luminance	Lv	If=110mA	--	100	--	cd/m^2

3.4 Power Supply



Mikrokontroler ATMega8535

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels for TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x for TQFP Package Only
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega8535L
  - 4.5 - 5.5V for ATmega8535
- Speed Grades
  - 0 - 8 MHz for ATmega8535L
  - 0 - 16 MHz for ATmega8535

ATMEL

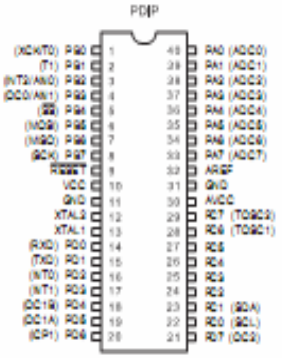
8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

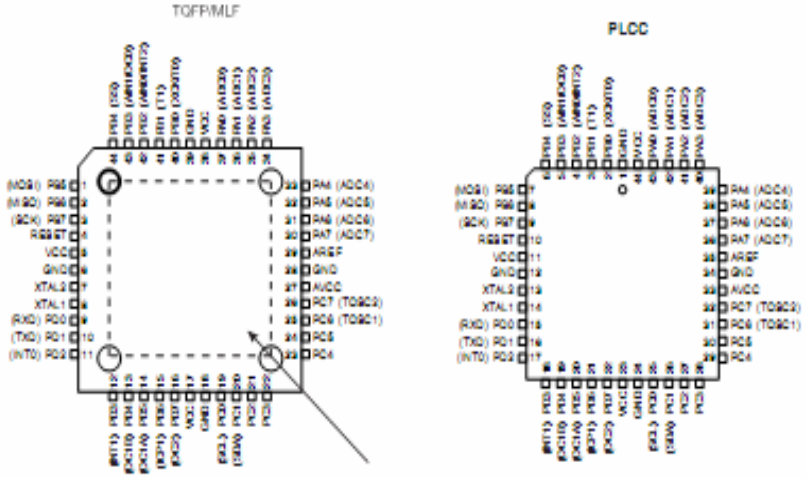
ATmega8535
ATmega8535L

Preliminary

Pin Configurations

Figure 1. Pinout ATmega8535





NOTE: MLF Bottom pad should be soldered to ground.

Disclaimer

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

8-bit Timer/Counter Register Description

Timer/Counter Control Register – TCCR0

Bit	7	6	5	4	3	2	1	0	
	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	TCCR0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – FOC0: Force Output Compare**

The FOC0 bit is only active when the WGM00 bit specifies a non-PWM mode. However, for ensuring compatibility with future devices, this bit must be set to zero when TCCR0 is written when operating in PWM mode. When writing a logical one to the FOC0 bit, an immediate Compare Match is forced on the Waveform Generation unit. The OC0 output is changed according to its COM01:0 bits setting. Note that the FOC0 bit is implemented as a strobe. Therefore it is the value present in the COM01:0 bits that determines the effect of the forced compare.

A FOC0 strobe will not generate any interrupt, nor will it clear the timer in CTC mode using OCR0 as TOP.

The FOC0 bit is always read as zero.

- **Bit 6, 3 – WGM01:0: Waveform Generation Mode**

These bits control the counting sequence of the counter, the source for the maximum (TOP) counter value, and what type of waveform generation to be used. Modes of operation supported by the Timer/Counter unit are: Normal mode, Clear Timer on Compare Match (CTC) mode, and two types of Pulse Width Modulation (PWM) modes. See Table 39 and "Modes of Operation" on page 74.

Table 39. Waveform Generation Mode Bit Description[1]

Mode	WGM01 (CTC0)	WGM00 (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

Note: 1. The CTC0 and PWM0 bit definition names are now obsolete. Use the WGM01:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the Timer.

- **Bit 5:4 – COM01:0: Compare Match Output Mode**

These bits control the Output Compare pin (OC0) behavior. If one or both of the COM01:0 bits are set, the OC0 output overrides the normal port functionality of the I/O pin it is connected to. However, note that the Data Direction Register (DDR) bit corresponding to the OC0 pin must be set in order to enable the output driver.

When OC0 is connected to the pin, the function of the COM01:0 bits depends on the WGM01:0 bit setting. Table 40 shows the COM01:0 bit functionality when the WGM01:0 bits are set to a normal or CTC mode (non-PWM).

Table 40. Compare Output Mode, non-PWM Mode

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Toggle OC0 on Compare Match
1	0	Clear OC0 on Compare Match
1	1	Set OC0 on Compare Match

Table 41 shows the COM01:0 bit functionality when the WGM01:0 bits are set to fast PWM mode.

Table 41. Compare Output Mode, Fast PWM Mode[1]

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Reserved
1	0	Clear OC0 on Compare Match, set OC0 at TOP
1	1	Set OC0 on Compare Match, clear OC0 at TOP

Note: 1. A special case occurs when OCR0 equals TOP and COM01 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Fast PWM Mode" on page 75 for more details.

Table 42 shows the COM01:0 bit functionality when the WGM01:0 bits are set to phase correct PWM mode.

Table 42. Compare Output Mode, Phase Correct PWM Mode[1]

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Reserved
1	0	Clear OC0 on Compare Match when up-counting. Set OC0 on Compare Match when down-counting.
1	1	Set OC0 on Compare Match when up-counting. Clear OC0 on Compare Match when down-counting.

Note: 1. A special case occurs when OCR0 equals TOP and COM01 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Phase Correct PWM Mode" on page 77 for more details.

- **Bit 2:0 – CS02:0: Clock Select**

The three Clock Select bits select the clock source to be used by the Timer/Counter.

Table 43. Clock Select Bit Description

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/counter stopped).
0	0	1	$clk_{I/O}$/(No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

If external pin modes are used for the Timer/Counter0, transitions on the T0 pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

Timer/Counter Register – TCNT0

Bit	7	6	5	4	3	2	1	0	
	TCNT0[7:0]								TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter Register gives direct access, both for read and write operations, to the Timer/Counter unit 8-bit counter. Writing to the TCNT0 Register blocks (removes) the Compare Match on the following timer clock. Modifying the counter (TCNT0) while the counter is running, introduces a risk of missing a Compare Match between TCNT0 and the OCR0 Register.

Output Compare Register – OCR0

Bit	7	6	5	4	3	2	1	0	
	OCR0[7:0]								OCR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Output Compare Register contains an 8-bit value that is continuously compared with the counter value (TCNT0). A match can be used to generate an output compare interrupt, or to generate a waveform output on the OC0 pin.

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 1 – OCIE0: Timer/Counter0 Output Compare Match Interrupt Enable**

When the OCIE0 bit is written to one, and the I-bit in the Status Register is set (one), the Timer/Counter0 Compare Match interrupt is enabled. The corresponding interrupt is executed if a Compare Match in Timer/Counter0 occurs (i.e., when the OCF0 bit is set in the Timer/Counter Interrupt Flag Register – TIFR).

Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-0.5V to V_{CC}+0.5V
Voltage on $\overline{\text{RESET}}$ with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	Except XTAL1 pin	-0.5		0.2 V_{CC}[1]	V
V_{IL1}	Input Low Voltage	XTAL1 pin, External Clock Selected	-0.5		0.1 V_{CC}[1]	V
V_{IH}	Input High Voltage	Except XTAL1 and $\overline{\text{RESET}}$ pins	0.6 V_{CC}[2]		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	XTAL1 pin, External Clock Selected	0.8 V_{CC}[2]		V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	$\overline{\text{RESET}}$ pin	0.9 V_{CC}[2]		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[3] (Ports A,B,C,D)	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.7 0.5	V V
V_{OH}	Output High Voltage[4] (Ports A,B,C,D)	I_{OH} = -20 mA, V_{CC} = 5V I_{OH} = -10 mA, V_{CC} = 3V	4.2 2.2			V V
I_{IL}	Input Leakage Current I/O Pin	V_{CC} = 5.5V, pin low (absolute value)			1	µA
I_{IH}	Input Leakage Current I/O Pin	V_{CC} = 5.5V, pin high (absolute value)			1	µA
R_{RST}	Reset Pull-up Resistor		30		60	kΩ
R_{pu}	I/O Pin Pull-up Resistor		20		50	kΩ

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted) (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Active 4 MHz, V_{CC} = 3V (ATmega8535L)		4		mA
		Active 8 MHz, V_{CC} = 5V (ATmega8535)		14		mA
		Idle 4 MHz, V_{CC} = 3V (ATmega8535L)		3		mA
		Idle 8 MHz, V_{CC} = 5V (ATmega8535)		10		mA
	Power-down mode[5]	WDT enabled, V_{CC} = 3V		< 10		µA
		WDT disabled, V_{CC} = 3V		< 3		µA
V_{ACIO}	Analog Comparator Input Offset Voltage	V_{CC} = 5V V_{in} = V_{CC}/2			40	mV
I_{ACLK}	Analog Comparator Input Leakage Current	V_{CC} = 5V V_{in} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog Comparator Propagation Delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low.
2. "Min" means the lowest value where the pin is guaranteed to be read as high.
3. Although each I/O port can sink more than the test conditions (20mA at V_{CC} = 5V, 10mA at V_{CC} = 3V) under steady stat conditions (non-transient), the following must be observed:
   PDIP Package:
   1] The sum of all IOL, for all ports, should not exceed 200 mA.
   2] The sum of all IOL, for port A0 - A7, should not exceed 100 mA.
   3] The sum of all IOL, for ports B0 - B7,C0 - C7, D0 - D7 and XTAL2, should not exceed 100 mA.
   TQFP Package:
   1] The sum of all IOL, for all ports, should not exceed 400 mA.
   2] The sum of all IOL, for ports A0 - A7, should not exceed 100 mA.
   3] The sum of all IOL, for ports B0 - B3, should not exceed 100 mA.
   4] The sum of all IOL, for ports B4 - B7, should not exceed 100 mA.
   5] The sum of all IOL, for ports C0 - C3, should not exceed 100 mA.
   6] The sum of all IOL, for ports C4 - C7, should not exceed 100 mA.
   7] The sum of all IOL, for ports D0 - D3 and XTAL2, should not exceed 100 mA.
   8] The sum of all IOL, for ports D4 - D7, should not exceed 100 mA.
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greate than the listed test condition.
4. Although each I/O port can source more than the test conditions (20mA at V_{CC} = 5V, 10mA at V_{CC} = 3V) under steady stat conditions (non-transient), the following must be observed:
   PDIP Package:
   1] The sum of all IOH, for all ports, should not exceed 200 mA.
   2] The sum of all IOH, for port A0 - A7, should not exceed 100 mA.
   3] The sum of all IOH, for ports B0 - B7,C0 - C7, D0 - D7 and XTAL2, should not exceed 100 mA.
   TQFP Package:
   1] The sum of all IOH, for all ports, should not exceed 400 mA.
   2] The sum of all IOH, for ports A0 - A7, should not exceed 100 mA.
   3] The sum of all IOH, for ports B0 - B3, should not exceed 100 mA.
   4] The sum of all IOH, for ports B4 - B7, should not exceed 100 mA.
   5] The sum of all IOH, for ports C0 - C3, should not exceed 100 mA.
   6] The sum of all IOH, for ports C4 - C7, should not exceed 100 mA.
   7] The sum of all IOH, for ports D0 - D3 and XTAL2, should not exceed 100 mA.
   8] The sum of all IOH, for ports D4 - D7, should not exceed 100 mA